Complete PoE Connected LED Driver Power Solution, IEEE 802.3bt NCL31010

Description

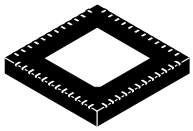
The NCL31010 is a member of the **onsemi** Power over Ethernet Powered Device (PoE−PD) product family and integrates an IEEE 802.3bt PoE−PD interface controller, a dual step−down converter and a buck convertor LED driver. The NCL31010 incorporates all the required functions for operation within a PoE system such as detection, classification and current limiting during the inrush phase. The NCL31010 contains synchronous step−down DC/DC converters for the main 3.3 V system supply as well as an auxiliary supply. In addition, the NCL31010 also integrates a current mode buck DC/DC controller designed to operate as a LED driver. The LED driver supports both PWM dimming and high−bandwidth analog dimming.

The NCL31010 supports high−power applications (up to 90 W PoE).

Features

- Fully Supports IEEE 802.3af/at and 802.3bt Specifications
- Assigned Power Level Up to 90 W
- Proprietary 100 W+ Applications
- Supports Autoclass
- HV Maintain Power PWM Output (MPS)
- Integrated 3.3 V Buck Convertor
- Integrated Adjustable Buck Convertor 2.5 – 24 V
- Integrated High Efficiency Buck LED Driver
- Adjustable Switching Frequency 44.4 kHz to 1 MHz
- Deep Dimming to Zero with Accuracy of 0.1% Using Internal Precision 2.4 V Reference
- Best in Class Linearity
- High Modulation Bandwidth (~50 kHz)
  - Visual Light Communication Capable
  - Yellow−Dot™ Compliant
- Internal DIM DAC for Independent LED Control During Micro−controller Re−flashing (Warm Boot)
- Low EMI Reference Design
- I^{2}C/SPI Interface (NCL31010I/NCL31010S)
- High Accuracy Diagnostic Functions to Measure Voltages/Currents
- Protection against LED Shorts & Opens
- LED Over/Under Voltage & Over Current Protection
- Chip Over Current Protection
- Chip & LED Over Temperature Protection
- Junction Temperature Range of −40°C to +125°C
- Available in 48−pin QFN 7x7
- These Devices are Pb−Free and are RoHS Compliant

RELATED STANDARDS
IEEE 802.3bt−2018



QFN48 7x7, 0.5P
CASE 485EP

MARKING DIAGRAM

NCL31010x = Specific Device Code (x = I, S)
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NCL31010MNITWG	QFN48	2500 / Tape & Reel
NCL31010MNSTWG	QFN48	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

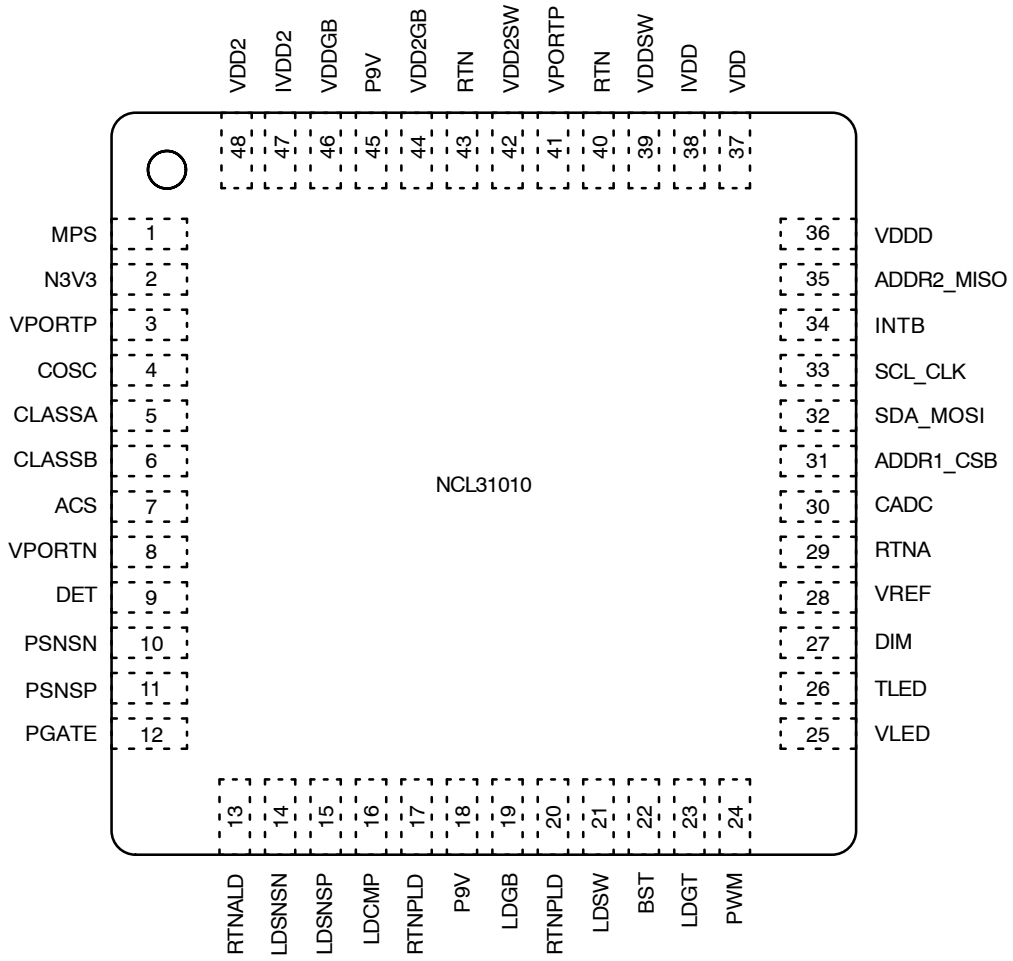


Figure 1. Pin−out NCL31010 in 48−pin QFN (Top View)

PIN DESCRIPTION

Pin No.	Signal Name	Type	Description
1	MPS	Output	Maintain Power Signature PWM output.
2	N3V3	Power	−3V3 LDO output. Decouple to VPORTP (pin 3) with a 1 μF capacitor.
3	VPORTP	Power	Positive input power. Connect to the positive terminal of the PoE rectifier bridge.
4	COSC	Analog	Connect a 1 nF 2% capacitor between COSC and VPORTN. This pin is pulled to VPORTP during the detection phase.
5	CLASSA	Output	Connect a class signature programming resistor to VPORTN. See classification section for recommended values.
6	CLASSB	Output	
7	ACS	Input	Autoclass enable/disable input. Pull to VPORTN to disable Autoclass; leave floating to enable Autoclass.
8	VPORTN	Power	Negative input power for PoE. Connect to the negative terminal of the PoE bridge rectifier.
9	DET	Open Drain	Connect a 26.1 kΩ detection resistor between DET and COSC. This pin is pulled to VPORTN during the detection phase.
10	PSNSN	Input	Negative input current sense line. Connect to VPORTN at the negative side of the external input current sense resistor.
11	PSNSP	Input	Positive input current sense line. Connect to the positive side of the external input current sense resistor.
12	PGATE	Output	Gate driver for the external pass transistor.

PIN DESCRIPTION (continued)

Pin No.	Signal Name	Type	Description
13	RTNALD	Power	Application ground. Connect to the drain of the external pass transistor. Return for the LED Buck compensation network.
14	LDSNSN	Input	Negative LED current sense line. Connect to the RTN side of LDSNS.
15	LDSNSP	Input	Positive LED current sense line. Connect to the positive side of LDSNS.
16	LDCOMP	Analog	Compensation pin for the LED driver.
17	RTNPLD	Power	Application ground. LED Buck power return.
18	P9V	Power	9 V gate drive voltage regulator output. Decouple to RTNPLD with a 1 μF capacitor. Connect to P9V (pin 45) with a trace on the PCB.
19	LDGB	Output	LED buck convertor bottom switch gate driver.
20	RTNPLD	Power	Application ground. LED Buck power return.
21	LDSW	Power	LED buck convertor switching node.
22	BST	Power	Boost voltage for top switch gate drive. Decouple to LDSW with a 100 nF capacitor.
23	LDGT	Output	LED buck convertor bottom switch gate driver.
24	PWM	Input	PWM Dimming input.
25	VLED	Input	LED string voltage measurement. Connect to RTN when not used.
26	TLED	Input	LED string NTC resistor divider measurement point. Connect to RTN when not used.
27	DIM	Analog	Analog Dimming input.
28	VREF	Analog	Reference precision voltage output. Decouple with a 2.2 μF capacitor.
29	RTNA	Power	Application ground. Analog return.
30	CADC	Analog	ADC filter capacitor connection. Decouple to RTNA with a 10 nF capacitor.
31	ADDR1_CSB	Input	I^2C Address for I^2C mode. Tie to RTN, VDDD or leave floating for alternative I^2C address. CSB in SPI mode.
32	SDA_MOSI	Input/Output	I^2C Data line. External pull−up resistor required. MOSI in SPI mode.
33	SCL_CLK	Input	I^2C Clock line. External pull−up resistor required. CLK in SPI mode.
34	INTB	Open Drain	I^2C Interrupt pin. External pull−up resistor required.
35	ADDR2_MISO	Input	I^2C Address. Tie to RTN or leave floating for alternative I^2C address. MISO in SPI mode.
36	VDDD	Power	3V3 power input for the NCL31010 digital circuitry.
37	VDD	Power	3V3 power output for the chip and external circuitry.
38	IVDD	Input	Current measurement for VDD regulator. Connect to the positive terminal of the VDD sense resistor.
39	VDDSW	Power	VDD buck convertor switching node.
40	RTN	Power	Application ground. Ground connection for the VDD and VDD2 DC/DC convertors.
41	VPORTP	Power	Positive input power. Decouple to the RTN with a 1 μF capacitor. Connect to the positive terminal of the PoE rectifier bridge.
42	VDD2SW	Power	VDD2 buck convertor switching node.
43	RTN	Power	Application ground. Ground connection for the VDD and VDD2 DC/DC convertors
44	VDD2GB	Output	VDD2 buck convertor bottom switch gate driver.
45	P9V	Power	9 V gate drive voltage input. Decouple to RTN with a 100 nF capacitor. Connect to P9V (pin 18) with a trace on the PCB.
46	VDDGB	Output	VDD buck convertor bottom switch gate driver.
47	IVDD2	Input	Current measurement for VDD2 regulator. Connect to the positive terminal of the VDD2 sense resistor.
48	VDD2	Power	VDD2 power output for external circuitry.

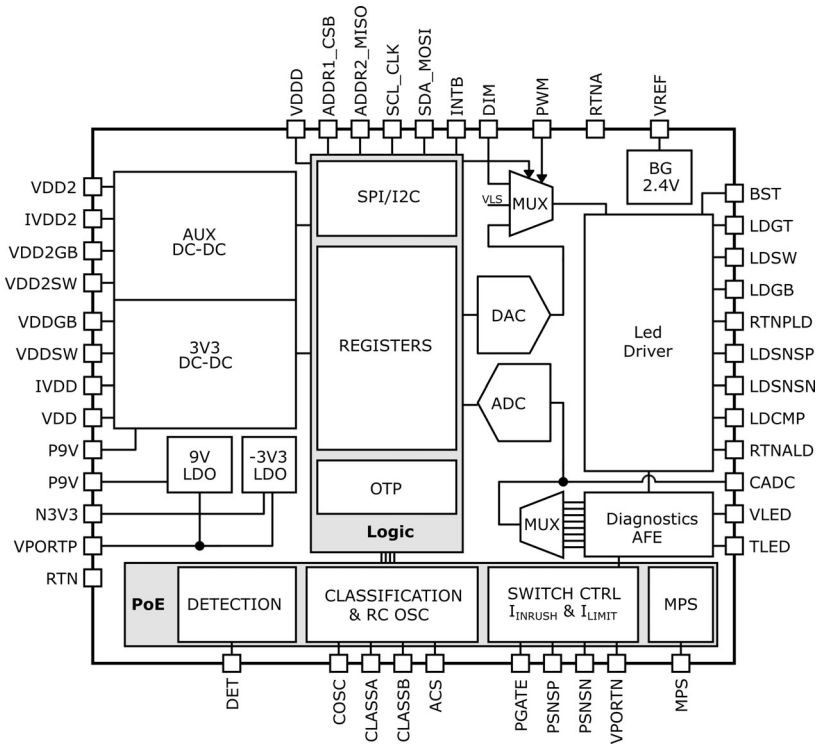


Figure 2. NCL31010 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VPORTP	Input Power Supply vs. VPORTN	−0.3	70	V
RTN, RTNPLD, RTNA, RTNALD	Application Ground vs. VPORTN	−0.3	VPORTP + 0.3	V
BST	Analog Output vs. LDSW	−0.3	11	V
LDGT	Analog Output vs. RTN	−0.3	Min (70, VPORTP + 11)	V
LDSW	Analog Output vs. RTN	−0.3	VPORTP+0.3	V
PSNSN, PSNSP	Analog Input vs. VPORTN	−0.3	3.6	V
DET	Analog Output vs. VPORTN			
PGATE	Analog Output vs. VPORTN	−0.3	11	V
COSC	Analog Input vs. VPORTN	−0.3	VPORTP + 0.3	V
CLASSA, CLASSB	Analog Output vs. VPORTN			
ACS	Analog Input vs. VPORTN			
LDSNSN, LDSNSP	Analog Input vs. RTN	−0.3	0.3	V
VDD	3.3 V Analog Supply vs. RTN	−0.3	3.6	V
VDDD	3.3 V Digital Supply vs. RTN			
ADDR1_CSB	Digital Input/Output vs. RTN			
ADDR2_MISO	Digital Input/Output vs. RTN			
VREF	Analog Output vs. RTN			
DIM	Analog Input vs. RTN			
CADC	Analog Output vs. RTN			
LDCOMP	Compensation Pin vs. RTN			

ABSOLUTE MAXIMUM RATINGS (continued)

Symbol	Parameter	Min	Max	Unit
IVDD	Analog Input vs. RTN	−0.3	Min (3.6, VDD + 0.3)	V
SDA_MOSI	Digital Input/Output vs. RTN	−0.3	5.5	V
SCL_CKL	Digital Input vs. RTN			
INTB	Open Drain Digital Output vs. RTN			
P9V	Analog Output vs. RTN	−0.3	11	V
VDDGB, VDD2GB	Analog Output vs. RTN			
LDGB	Analog Output vs. RTN			
N3V3	Analog Output vs. RTN	VPORTP − 3.6	VPORTP + 0.3	V
MPS	MPS vs. VPORTN	−0.3	VPORTP + 0.3	V
VDD2	Analog Input vs. RTN	−0.3	VPORTP + 0.3	V
VLED	HV Tolerant Input vs. RTN			
PWM	HV Tolerant Input vs. RTN			
TLED	HV Tolerant Input vs. RTN			
IVDD2	Analog Input vs. RTN			
VDDSW	Analog Output vs. RTN	−0.6	VPORTP + 11	V
VDD2SW	Analog Output vs. RTN			
T_{STRG}	Storage Temperature	−55	+150	°C
T_J	Junction Temperature	−40	+125	°C
ESD−HBM	Human Body Model; EIA−JESD−A114	2	−	kV
ESD−CDM	Charged Device Model; ESD−STM5.3.1	500	−	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{PORT}	Input Power Supply (V_{PORT} = V_{PORTP} − V_{PORTN})	−	57	V
V_{I_D}	Digital Inputs SCL, SDA, INTB, PWM vs. RTN	0	5	V
VTLED	Temperature Sense Analog Input vs. RTN	0	VDD	V
T_A	Ambient Temperature	−40	+85	°C
T_J	Junction Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
θJC	Thermal Resistance, Junction−to−Case	38	°C/W
θJA	Thermal Resistance, Junction−to−Air	128	°C/W

1. θJA is obtained with 1S1P test board (1 signal − 1 plane) and natural convection. Refer to JEDEC JESD51 for details

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DETECTION CHARACTERISTICS						
Rdetect	Equivalent Detection Resistance	R_{DET} = 26.1 kΩ ±1% 1 V ≤ V_{PORT} ≤ 10.1 V	23.7	–	26.3	kΩ
VoffsetIC	Detection Offset Voltage (IC Part)		–	–	0.2	V
CLASSIFICATION CHARACTERISTICS						
Vcl_th	Class/Mark Current Switchover Threshold (Note 2)	V_{PORT} rising or falling	10.1	–	12.5	V
Vcldis	Classification Current Disable Threshold (Note 2)	V_{PORT} rising or falling	20.5	–	24.5	V
Iclsigq	Quiescent Current During Classification	V_{PORT} = 12.5 V	–	275	–	μA
Vcsr	CLASS Driver Voltage (Note 2) During Class Event	12.5 V ≤ V_{PORT} ≤ 20.5 V	8.5	9.15	9.7	V
Iclsig0	RclassA,B = 4.5 kΩ ±1%	12.5 V ≤ V_{PORT} ≤ 20.5 V	1	–	4	mA
Iclsig1	RclassA,B = 909 Ω ±1%	12.5 V ≤ V_{PORT} ≤ 20.5 V	9	–	12	mA
Iclsig2	RclassA,B = 511 Ω ±1%	12.5 V ≤ V_{PORT} ≤ 20.5 V	17	–	20	mA
Iclsig3	RclassA,B = 332 Ω ±1%	12.5 V ≤ V_{PORT} ≤ 20.5 V	26	–	30	mA
Iclsig4	RclassA,B = 232 Ω ±1%	12.5 V ≤ V_{PORT} ≤ 20.5 V	36	–	44	mA
Imark	IPORTP During Mark Event Range	V_{PORT} = 10.1 V	1	2.3	4	mA
tfce	Short/Long First Class Event Threshold	R_{DET} = 26.1 kΩ ±1%; C_{OSC} = 1 nF ±2%	75	–	88	ms
tacspd	Change to Class Signature ‘0’ Current Timing	Autoclass enabled	75.5	–	87.5	ms
RC OSCILLATOR CHARACTERISTICS						
fosc	Frequency of the Oscillator	R_{DET} = 26.1 kΩ; C_{OSC} = 1 nF	–	26.8	–	kHz
duty	Oscillator Duty Cycle		–	50	–	%
PASS SWITCH CURRENT CONTROL CHARACTERISTICS						
Iinr	Inrush Current	100 mΩ Sense Resistor	75	97.3	125	mA
Vdrain_pg	RTN PowerGood Threshold Voltage (Note 2)	RTN – VPORTN falling	0.9	1.0	1.1	V
Vgate_pg	PGATE PowerGood Threshold Voltage (Note 2)	PGATE – VPORTN rising	6.9	8.5	10.0	V
PASS SWITCH ON−STATE CHARACTERISTICS						
Ioc	Over Current Detection Level	100 mΩ Sense Resistor	5.4	6.0	6.7	A
Voc	RTN Overcurrent Detection Voltage (Note 2)	RTN – VPORTN rising	1.1	1.2	1.3	V
UNDER VOLTAGE LOCK−OUT CHARACTERISTICS						
UVLO_H	VPORT UVLO Threshold Voltage (Note 2)	V_{PORT} rising	33	35.1	37.5	V
UVLO_L	VPORT UVLO Threshold Voltage (Note 2)	V_{PORT} falling	30	32.3	34.5	V
UVLO_hyst	UVLO Threshold Hysteresis		2.4	2.8	3.3	V
PoE RESET CHARACTERISTICS						
Vrst	VPORT Reset Threshold Voltage (Note 2)	V_{PORT} falling	2.81	3.85	4.9	V
PASS SWITCH OFF−STATE CHARACTERISTICS						
Idd_off	Power−off Current (Note 3)	V_{PORT} = 57 V	–	260	–	μA
THERMAL PROTECTION CHARACTERISTICS						
TSD_PoE	Thermal Shutdown Threshold	Junction temperature	150	–	–	°C

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
MAINTAIN POWER TIMER						
Tclk_MPT	Timer Clock Cycle Period		972	1024	1076	μs
CONSUMPTIONS (V_{PORT} = 53 V)						
Idd_on,0	Operating Current	CTRL = 0; VDD Non−switching	–	2.03	–	mA
Idd_on,1	Operating Current w. VDD2	CTRL = 1; VDD, VDD2 Non−switching	–	2.12	–	mA
Idd_on,2	Operating Current w. Metrology	CTRL = 4; VDD Non−switching	–	2.06	–	mA
Idd_on,3	Operating Current w. VDD2 & Metrology	CTRL = 5; VDD, VDD2 Non−switching	–	2.15	–	mA
VDD & VDD2 DCDC ELECTRICAL SPECIFICATIONS						
VDDx_Freq	Switching Frequency	JIT_EN = 0	126.6	133.3	140	kHz
N3V3	Internal VPORTP−N3V3 Voltage	0 ≤ I ≤ 5 mA	3.13	3.3	3.47	V
P9V	Internal P9V Voltage (Generated in LED Block)	0 ≤ I ≤ 20 mA	8.55	9	9.45	V
VDDxGB_Rpu	LS Gate Driver Pull−up Resistance		15	28	65	Ω
VDDxGB_Rpd	LS Gate Driver Pull−down Resistance		2	3.25	6.5	Ω
VDDxGB_Tr	LS Gate Driver Rise Time		10	20	52	ns
VDDxGB_Tf	LS Gate Drive Fall Time		3	6	16	ns
VDD MAIN DCDC ELECTRICAL SPECIFICATIONS						
DC3V3_VDD	Main Supply Output Voltage		3.234	3.3	3.366	V
DC3V3_ILMT	Peak Inductor Current Limit	R_{sns} = 0.75 Ω	230	300	370	mA
VDD_Ton,min	Minimum ON Time		50	110	200	ns
VDD_Toff,min	Minimum OFF Time		50	88	200	ns
VDD_HS_Ron	Top Switch on Resistance		1.5	3.3	7.5	Ω
I_VDDD	Operating Current on VDDD	CTRL = 0	–	3.15	–	mA
VDD_ACRp	Equivalent AC Parallel Resistance	R_{sns} = 0.75 Ω; CCM	–	0.6	–	Ω
VDD_ACLp	Equivalent AC Parallel Inductance	R_{sns} = 0.75 Ω; CCM	–	149	–	μH
VDDD RESET ELECTRICAL SPECIFICATIONS						
VDD_POR_LH	VDD(D) Reset Threshold H	VDD(D) Rising	2.8	2.9	3.05	V
VDD_POR_HL	VDD(D) Reset Threshold L	VDD(D) Falling	2.5	2.7	2.8	V
VDD_POR_HY	VDD(D) Reset Hysteresis		0.2	0.3	0.4	V
VDD2 AUXILIARY DCDC ELECTRICAL SPECIFICATIONS						
DCAUX_VDD2	Aux Supply Output Voltage	5V0 (VDD2_SEL = 2)	4.9	5	5.1	V
		7V2 (VDD2_SEL = 6)	7.056	7.2	7.344	V
		2V5 (VDD2_SEL = 0)	2.45	2.5	2.55	V
		3V3 (VDD2_SEL = 4)	3.234	3.3	3.366	V
		10V (VDD2_SEL = 1)	9.8	10	10.2	V
		12V (VDD2_SEL = 5)	11.76	12	12.24	V
		15V (VDD2_SEL = 3)	14.7	15	15.3	V
		24V (VDD2_SEL = 7)	23.52	24	24.48	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DCAUX_ILMT	Peak Inductor Current Limit	5V0; R_{sns} = 0.22 Ω	882	948	1014	mA
		7V2; R_{sns} = 0.22 Ω	601	668	750	mA
		2V5; R_{sns} = 0.20 Ω	811	872	933	mA
		3V3; R_{sns} = 0.20 Ω	802	862	922	mA
		10V; R_{sns} = 0.33 Ω	544	604	664	mA
		12V; R_{sns} = 0.33 Ω	544	604	664	mA
		15V; R_{sns} = 0.33 Ω	538	598	678	mA
		24V; R_{sns} = 0.36 Ω	450	547	650	mA
VDD2_Ton,min	Minimum ON Time		50	87	150	ns
VDD2_Ton,min	Minimum OFF Time		50	84	150	ns
VDD2_HS_Ron	Top Switch on Resistance		0.5	1.1	2.65	Ω
VDD2_Sx	Slope Compensation	15V; R_{sns} = 0.33 Ω	–	0.073	–	A/μs
		24V; R_{sns} = 0.36 Ω	0.028	0.067	–	A/μs
VDD2_ACRp	Equivalent AC Parallel Resistance	5V0; R_{sns} = 0.22 Ω; CCM	–	0.23	–	Ω
		7V2; R_{sns} = 0.22 Ω; CCM	–	0.53	–	Ω
		2V5; R_{sns} = 0.20 Ω; CCM	–	0.12	–	Ω
		3V3; R_{sns} = 0.20 Ω; CCM	–	0.15	–	Ω
		10V; R_{sns} = 0.33 Ω; CCM	–	1.22	–	Ω
		12V; R_{sns} = 0.33 Ω; CCM	–	1.16	–	Ω
		15V; R_{sns} = 0.33 Ω; CCM	–	0.92	–	Ω
		24V; R_{sns} = 0.36 Ω; CCM	–	2.09	–	Ω
VDD2_ACLp	Equivalent AC Parallel Inductance	5V0; R_{sns} = 0.22 Ω; CCM	–	60	–	μH
		7V2; R_{sns} = 0.22 Ω; CCM	–	120	–	μH
		2V5; R_{sns} = 0.20 Ω; CCM	–	29	–	μH
		3V3; R_{sns} = 0.20 Ω; CCM	–	38	–	μH
		10V; R_{sns} = 0.33 Ω; CCM	–	275	–	μH
		12V; R_{sns} = 0.33 Ω; CCM	–	275	–	μH
		15V; R_{sns} = 0.33 Ω; CCM	–	229	–	μH
		24V; R_{sns} = 0.36 Ω; CCM	–	514	–	μH

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min	Typ	Max	Unit
LED DRIVER ELECTRICAL SPECIFICATIONS					
VPORTP	Input Voltage Range for Stable Output	24	–	57	V
VLED	LED String Voltage vs. RTN	4	–	38	V
VDIM	Analog DIM Input vs. RTN	0	–	2.4	V
ILED (Note 4)	LED Current Range	0	–	3	A
VSNS (Note 5)	Sense Resistor Voltage	−0.024	–	0.3	V
VCSA_0 (Note 6)	Sense Amplifier Output Voltage [Inputs Shorted]	199.05	201	202.95	mV
ILED_OFFS (Note 7)	LED Current Regulation Offset Error Relative to VREF	−0.081	–	0.081	%
ILED_GAIN (Note 8)	LED Current Regulation Gain Error	−2	–	2	%
LED DRIVER SAWTOOTH SLOPE COMPENSATION ELECTRICAL SPECIFICATIONS					
SLP1_1	Slope Compensation 1 with SLP1<1:0> = 00	0.07	0.1	0.13	V/μs
SLP1_2	Slope Compensation 1 with SLP1<1:0> = 01	0.14	0.2	0.26	V/μs
SLP1_3	Slope Compensation 1 with SLP1<1:0> = 10	0.21	0.3	0.39	V/μs
SLP1_4	Slope Compensation 1 with SLP1<1:0> = 11	0.28	0.4	0.52	V/μs
SLP2_1	Slope Compensation 2 with SLP2<1:0> = 00	0.21	0.3	0.39	V/μs
SLP2_2	Slope Compensation 2 with SLP2<1:0> = 01	0.28	0.4	0.52	V/μs
SLP2_3	Slope Compensation 2 with SLP2<1:0> = 10	0.42	0.6	0.78	V/μs
SLP2_4	Slope Compensation 2 with SLP2<1:0> = 11	0.63	0.9	1.17	V/μs
LED DRIVER INTERNAL DAC ELECTRICAL SPECIFICATIONS					
DIM_DNL	Internal DIM Differential Nonlinearity	−0.5	0	0.5	LSB
DIM_INL	Internal DIM Integral Nonlinearity	−0.5	0	0.5	LSB
DIM_MAX	Internal DIM Maximum (Code 0x7F)	2.376	2.4	2.424	V
DIM_MIN	Internal DIM Minimum (Code 0x09)	–	187.5	–	mV
DIM_RES	Internal DIM DAC Resolution	–	7	–	LSB
LED DRIVER OVER−CURRENT PROTECTION ELECTRICAL SPECIFICATION					
OCP_TH	Comparator Threshold	–	382	–	mV
LED DRIVER SOFT−START /OTA/NON−OVERLAPPING ELECTRICAL SPECIFICATION					
GM	Error Amplifier Transconductance gm in Operational Mode	0.5	1	1.5	mS
GM_SST	Error Amplifier Transconductance gm in Soft Start Mode	60	100	180	μS
TOFF_MIN	Minimum ON Time of the LS and HS Driver	10	25	50	ns
TNOV	Non−overlapping Time	10	25	50	ns
REFERENCE VOLTAGE CHARACTERISTICS					
VREF	Voltage Reference for DIAG/LED/DCDC [IREF < 2 mA]	2.394	2.4	2.406	V
IREF	Voltage Reference Current Consumption	–	–	2	mA
I^2C TIMING CHARACTERISTICS (NCL31010I)					
f_SCL	Interface Clock Frequency	–	–	400	kHz
SPI TIMING CHARACTERISTICS (NCL31010S)					
f_SCLK	Interface Clock Frequency	–	–	2	MHz

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min	Typ	Max	Unit
DIAGNOSTICS ELECTRICAL SPECIFICATION					
DIAG_ILED	LED Current Measurement Overall Accuracy	−0.6	–	0.6	%
DIAG_VLED	LED Voltage Measurement Overall Accuracy	−0.5	–	0.5	%
DIAG_IPORT	Input Current Measurement Overall Accuracy	−1	–	1	%
DIAG_VPORT	Input Voltage Measurement Accuracy	−0.7	–	0.7	%
DIAG_IVDD	VDD Current Measurement Overall Accuracy	−2	–	2	%
DIAG_IVDD2	VDD2 Current Measurement Overall Accuracy	−2	–	2	%
DIAG_VDD	VDD Voltage Measurement Overall Accuracy	−1	–	1	%
DIAG_VDD2	VDD2 Voltage Measurement Overall Accuracy	−1	–	1	%
DIAG_TLED	TLED Voltage Measurement Overall Accuracy	−1	–	1	%
DIAG_CONSO	DIAG Current Consumption	–	–	200	μA
THERMAL PROTECTION CHARACTERISTICS					
TSD_H	Thermal Shutdown, High Threshold	141	150	159	°C
TSD_L	Thermal Shutdown, Low Threshold	126.9	135	143.1	°C
TWRN_H	Thermal Warning, High Threshold	112.8	120	127.2	°C
TWRN_L	Thermal Warning, Low Threshold	101.5	108	114.5	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Voltage referenced to VPORTN
3. E.g. after overcurrent timeout
4. This range depends on the sense resistor RSNS.
5. Assume inductor current ripple included. This spec implies that the inductor current ripple size has an upper limit VSNSmin > RSNS x Ippmax / 2.
6. The VCSA voltage is the output of the LED sense amplifier and is the compare voltage for the DIM input. VCSA_0 is given with the inputs shorted. The VCSA_0 voltage is the threshold to get exactly zero current.
7. This deviation is the total offset in the DIM versus LED current relationship. It is specified relative to the VREF typical. It is useful for calculating the maximum offset error when using a VREF based solution for accurate dimming to low currents.
8. This error is a dominant factor in the LED current regulation error at mid and high LED currents. It is specified relative to VREF typical. Assume RSNS = 100 mΩ and ideal.

SIMPLIFIED APPLICATION SCHEMATIC

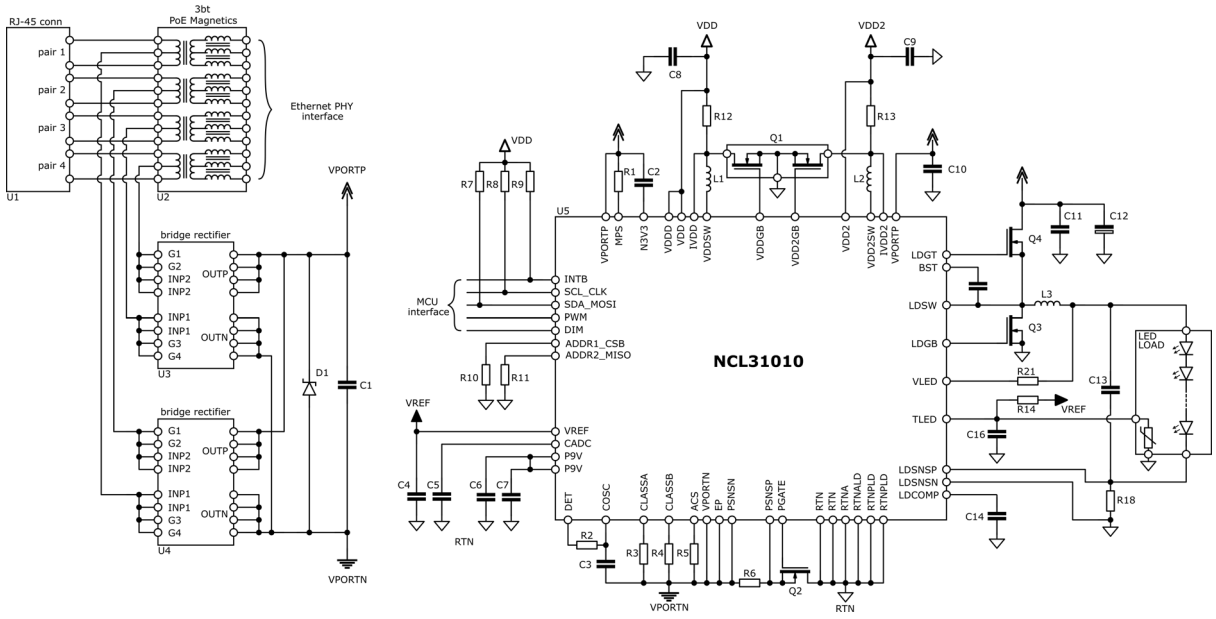


Figure 3. Typical Application Schematic

Table 1. TYPICAL BILL OF MATERIALS

Symbol	Description	Value	Rating	Remark	Reference
D1	TVS Protection, unidirectional	58 V_{RSo}			SMBJ58A
C1	Decoupling	100 nF	100 V		0805B104K101C
C2	Decoupling, buffer	1 μF	25 V		C0603C105K3PACTU
C3	RC oscillator	1 nF/2%	25 V		GRM1885C1H102GA01
C4	Decoupling	2.2 μF	10 V		C0603C225K8RACTU
C5	Sample and Hold for ADC	10 nF	25 V		C0603C103K3RACTU
C6	Decoupling, buffer	1 μF	25 V		C0603C105K3PACTU
C7	Decoupling	100 nF	25 V		C0603C104K3RACTU
C8	Output capacitor for VDD	22 μF	6.3 V	*	C1206C226K9PAC
C9	Output capacitor for VDD2	47 μF	6.3 V	*	C1210C476M9PAC
C10	Fast filter capacitor for DC−DC's and chip	1 μF	100 V		C1210C105K1RAC
C11	Fast filter capacitor for LED driver	2 x 1 μF	100 V	(Note 12)	C1210C105K1RACTU
C12	Buffer capacitor for application	56 μF	80 V	*	A759MS566M1KAAE045
C13	LED driver output capacitors	2 x 470 nF	100 V	(Note 12)	C0805C471K1RACTU
C14	LED driver compensation capacitor	10 nF	25 V		C0603C103K3RACTU
C16	Filtering TLED	100 nF	25 V		C0603C104K3RACTU
R1	MPS resistor	3.09 kΩ	1 W	*	ERJ−1TNF3091U
R2	PoE detection	26.1 kΩ	1%		RC0603FR−0726K1L
R3	PoE classification	232 Ω	1%	(Note 9)	ERJ8ENF2320V
R4	PoE classification	332 Ω	1%	(Note 9)	ERJ6ENF3320V
R5	Auto−classification resistor	0 Ω		*	
R6	PoE current limiting & sense resistor for diagnostics	100 mΩ	3 W	(Note 11)	CRA2512−FZ−R100ELF

Table 1. TYPICAL BILL OF MATERIALS (continued)

Symbol	Description	Value	Rating	Remark	Reference
R7	I^2C pull−up	4.7 kΩ			
R8	I^2C pull−up	4.7 kΩ			
R9	Interrupt pull−up	4.7 kΩ			
R10	I^2C address selection	0 Ω		*	
R11	I^2C address selection	0 Ω		*	
R12	VDD sense resistor	750 mΩ		(Note 11)	RCWE0603R750FKEA
R13	VDD2 sense resistor	200 mΩ		(Note 11)	RL1220S−R20−F
R18	LED driver current sense resistor	100 mΩ	1 W	(Note 10) (Note 11)	
R21	Protection resistor for overvoltage on VLED node	100 Ω			RC0603FR−07100RL
L1	VDD buck inductor	390 μH			744777239
L2	VDD2 buck inductor	100 μH			7447714101
L3	LED driver buck inductor	68 μH	3 A_{rms}	(Note 10) (Note 12)	
Q1	Dual NMOS bottom switching transistor for DC/DCs				FDC8602
Q2	Pass switch between VPORTN and RTN domains				FDMC8622
Q3	NMOS bottom switching transistor for LED driver				FDMA037N08L
Q4	NMOS top switching transistor for LED driver				NVTFS6H880N
U1	Shielded or unshielded Ethernet RJ−45 connector				
U2	3bt PoE Magnetics				
U3	Rectification bridge				FDMQ8205
U4	Rectification bridge				FDMQ8205
U5	Integrated PoE PD with LED driver and dc−dc's				NCL31010

9. Resistance value determines the requested power class.
10. Inductor and LED current sense resistor depend on the application specifications such as required power, allowed current ripple. See LED driver section for details.
11. The accuracy of the sense resistors is not considered in the specification of the current sense accuracy.
12. Saturation current >3.5 A
13. The values for L2, R13 and C9 in the table are specific for the 5 V VDD2 output. Refer to table 14 and 18 for other VDD2 output voltages.
14. The schematic does not show EMI filtering required for some applications.

POE FUNCTIONAL DESCRIPTION

The NCL31010 incorporates a Power over Ethernet Powered Device (PD) interface controller with an external n−channel MOSFET load switch.

Powered Device Interface

The NCL31010 is located at the interface of the PD and will interact with the Power Sourcing Equipment (PSE) over the Ethernet cable. NCL31010 allows the device to be powered by an IEEE 802.3af/at or −3bt compliant PSE. It provides a detection signature, classification handshaking, inrush current limitation and operational overcurrent protection. A block diagram is shown in Figure 2. Each section will be explained in more detail below.

Detection

During the detection phase, the PSE will check if a valid or a non−valid detection signature is present. This will enable the PSE to differentiate between equipment supporting PoE requesting power and equipment either not supporting PoE or not requesting power. In order to be able to present a valid detection signature to the PSE, a 26.1 kΩ resistor must be inserted between the COSC and DET pins of NCL31010. During the detection phase all blocks of the chip are in power−down except for an internal reference, a comparator and two switches.

When the voltage at the PD power interface is within the detection range, the COSC pin is pulled to VPORTP and the DET pin is pulled to VPORTN, resulting in the PD presenting a valid detection signature. The offset voltage of the input rectifier bridge should be between 0 and 1.7 V in the detection range (2.7 V ≤ V_{PD} ≤ 10.1 V).

When the PSE has detected a valid detection signature and continues towards powering on the PD, the COSC and DET switches are turned off in order to reduce the current consumption of the PD.

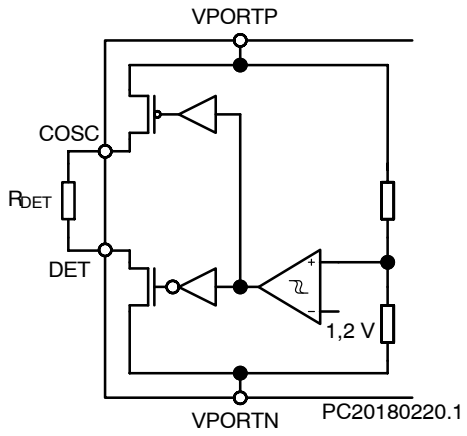


Figure 4. Detection Circuit

Classification

A PD is characterized based upon the maximum power level it requires at its power interface during operation. The IEEE 802.3bt standard supports up to 71.3 W PDs and defines 8 power Classes: Class 1 up to Class 8. The PD must conform to a Class with a power level that is at or above the maximum power the PD requires. Table 2 lists the different Classes and the corresponding power level they stand for. Based on the Class the PD conforms to, two resistance values are listed. The R_{classA} value must be inserted between CLASSA and VPORTN. Likewise, the R_{classB} value must be inserted between CLASSB and VPORTN. Eventually, when implementing a Class 1, 2, 3 or 4 PD, the CLASSA and CLASSB pins can be shorted together to the same single resistor.

Table 2. CLASSIFICATION RESISTOR VALUE

PD Class	PD Power	R_{CLASSA} (Note 16)	R_{CLASSB} (Note 16)
0 (Note 15)	*13 W*	*4.5 kΩ*	*4.5 kΩ*
1	3.84 W	909 Ω	909 Ω
2	6.49 W	511 Ω	511 Ω
3	13 W	332 Ω	332 Ω
4	25.5 W	232 Ω	232 Ω
5	40.0 W	232 Ω	4.5 kΩ
6	51.0 W	232 Ω	909 Ω
7	62.0 W	232 Ω	511 Ω
8	71.3 .. 90 W	232 Ω	332 Ω

15. 3bt compliant PDs should use Class 1, 2 or 3 instead of Class 0
16. All resistors must be 1% accurate

Once the PSE device has detected the PD device, the classification process begins. The NCL31010 is fully capable of responding and completing classification with all PSE types described in the 802.3af/at and −3bt PoE Standard. The Class requested by NCL31010 during classification is determined by the resistors connected to the CLASSA and CLASSB pins. Depending on the power the PSE is able to deliver to the PD, the PSE will generate a different number of class−mark events. This will determine the amount of power the PD is allowed to use. Next to that, the NCL31010 is able to distinguish between a 3bt compliant PSE and a 3af/at compliant PSE. Therefore a 1 nF capacitor must be inserted between COSC and VPORTN. The classification results will be written to the Classification Result Register (&CCR 0x03). The offset voltage of the input rectifier bridge should be between 0 and 2 V in the detection range (14.5 V ≤ V_{PD} ≤ 20.5 V).

During a class event, the power dissipation in the R_{class} resistor can be significant (V_{csr}^2 / R_{class}) and its package size must be chosen properly. When the port voltage rises above V_{cldis} the class drivers will be disabled in order to limit the power dissipation.

Inrush Current Limiting

When the PSE has successfully assigned the PD to a specific Class in correspondence with the power the PSE is able to deliver, the PSE will increase the voltage at its power interface up to its internal power supply voltage. NCL31010 will enter the inrush current control state once its port voltage rises above the UVLO_H threshold.

In this state, NCL31010 will control the charging of its port capacitance C_{PD} located between VPORTP and RTN by operating the pass switch transistor in the active region. The current through the pass switch is regulated by monitoring the voltage over an external sense resistor R_{SNS} = 100 mΩ. NCL31010 will limit the inrush current well below the PSE inrush threshold while charging its port capacitance. The nominal level of the inrush current is 97.3 mA typ. The NCL31010 will exit the inrush current control state when the voltage between RTN and VPORTN is smaller than 1.0 V and the gate voltage rises above 8.5 V. At this stage, the port capacitance can be considered to be fully charged, and NCL31010 will enter the normal operation mode with the pass switch completely turned on.

If the port capacitance voltage remains low due to an output short error condition, the inrush current control state will be aborted to protect the pass−switch. In order not to be considered as a short, the port capacitance should be chosen not to have too high a value (above 1.5 mF).

Class 1 and 2 PDs should operate according to their power Class 50 ms after the UVLO_H threshold was crossed. Therefore it is recommended to limit the port capacitance to 57 μF for Class1 PDs and to 77 μF for Class2 PDs.

System Start−up

Once NCL31010 exits the inrush current control state, it will set the PGOOD bit in the CRR register, indicating the VDD 3V3 DC/DC converter − and eventually the system − is allowed to start. This also indicates NCL31010 will no longer actively limit the current and/or the power, as the pass switch is on and will be left turned on.

PDs requesting Class 4 or higher need to take into account that they can be underpowered and need to implement some basic functionality with Class 3 power level. Also, the microcontroller will only be able to read the classification result after system startup. Therefore the VDD 3V3 DC/DC converter and the system must be able to start up with Class 3 power (or lower for Class 1 and Class 2 PDs) and turn on higher power loads only if this is allowed by the PSE assigned Class.

Even when being assigned to Class 4 or higher by the PSE, the PD is only allowed to use this increased power level 80 ms after the UVLO_H threshold was crossed. The nominal delay introduced to charge the port capacitance can be calculated from the formula below.

$$t_{charge}\ (ms) = \frac{C_{pd}\ (\mu F) \times V_{pd}\ (V)}{91} \qquad \text{(eq. 1)}$$

As an example, it typically takes 80 ms to charge a 145 μF capacitor to 50 V. Depending mainly on the chosen port capacitor value, this 80 ms delay may or may not yet have passed when the NCL31010 exits the inrush current control state.

CLASSEVENT Indicators

The state of the CLASSEVENT bits in the Classification Result Register (&CRR 0x03) provides information about the power level that the PSE has assigned to the PD during classification. These status bits are actually only relevant for PDs requesting Class 4 or higher as those need to take into account that they can be underpowered. See table 3 to determine the assigned power based on the CLASSEVENT bits and the requested Class. An underpowered PD can eventually be assigned to Class 3, 4 or 6.

Table 3. CLASSIFICATION RESULT OVERVIEW

Requested Class	CLASSEVENT Bit [1:0]	Assigned Class	Assigned Power
4	00b	3	13 W
	01b	4	25.5 W
	1Xb		
5	00b	3	13 W
	01b	4	25.5 W
	1Xb	5	40 W
6	00b	3	13 W
	01b	4	25.5 W
	1Xb	6	51 W
7	00b	3	13 W
	01b	4	25.5 W
	10b	6	51 W
	11b	7	62 W
8	00b	3	13 W
	01b	4	25.5 W
	10b	6	51 W
	11b	8	71.3..90 W

PDs assigned to Class 8 may consume greater than 71.3 W as long as they guarantee not to exceed the 90 W power limit at the PSE power interface. Operation beyond 71.3 W is, however, only possible if additional information is available to the PD regarding the actual link section DC resistance between the PSE and the PD.

The application should always operate at or below the assigned power limit. Failing to do so will result in the PSE disconnecting the PD.

LCF Indicator

The state of the LCF bit in the Classification Result Register (&CRR 0x03) provides information (retrieved during classification) about the type of PSE the PD is connected to:

Table 4. TYPE RESULT OVERVIEW

LCF Bit 2	PSE Categorization
0b	802.3af/at (PSE Type 1 or Type 2)
1b	802.3bt (PSE Type 3 or Type 4)

Maintain Power Signature

There is a minimum amount of current a PD needs to draw in order to allow the PSE to determine if the PD is still connected. This is called the Maintain Power Signature (MPS). If the PD no longer maintains this, the PSE may disconnect the power.

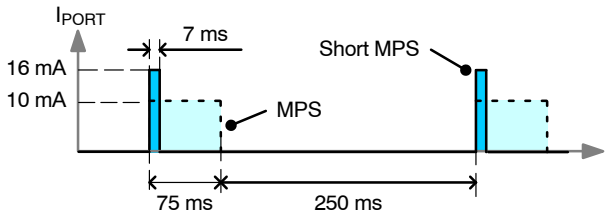


Figure 5. MPS

The current needs to be at or above a certain current threshold ($I_{Port\_MPS,Min}$) during at least a certain amount of time ($T_{MPS\_PD,Min}$). If this has been the case, the current may fall below the threshold for at most a certain dropout period ($T_{MPDO\_PD,Max}$).

Whether or not the lower power short MPS may be used depends upon the state of the LCF bit in the Classification Result Register (&CRR 0x03).

Table 5. MPS TIMING

LCF Bit 2	$T_{MPS\_PD,Min}$	$T_{MPDO\_PD,Max}$
0b	75 ms	250 ms
1b	7 ms	310 ms

For PDs requesting Class 4 or less the MPS current threshold will always be 10 mA.

For PDs requesting Class 5 or above the MPS current threshold will depend upon the assigned Class.

Table 6. MPS CURRENT

Assigned Class	$I_{Port\_MPS,Min}$
≤4	10 mA
≥5	16 mA

An important remark is that the PD load current will be low−pass filtered by its port capacitance and the actual resistance of the cable. This should be taken into account when generating current pulses for MPS.

The PD needs to maintain the MPS as soon as its port voltage rises above the UVLO_H threshold. Depending on the amount of port capacitance and the type of PSE it is connected to, the time duration of the inrush current control state might or might not be enough ($T_{MPS\_PD,Min}$) to count as the first valid current pulse. In combination with 3bt PSEs this will usually not be a problem as it typically takes 7 ms to charge just a 12.7 μF cap to 50 V. In combination with 3af/at PSEs the situation is different as it typically takes 75 ms to charge a 154 μF cap to 44 V.

Maintain Power Timer

The NCL31010 can generate a PWM waveform on the MPS pin to provide a Maintain Power Signature (MPS) and yet optimize the standby MPS power draw.

The Maintain Power Timer clock has a 1024 μs cycle period. The PWM output on MPS pin will consecutively remain low during N_{MPON} clock cycles and remain floating during N_{MPOFF} clock cycles; both numbers depend upon the state of the LCF bit in the Classification Result Register (&CRR 0x03):

Table 7. NUMBER OF CYCLES

LCF Bit 2	N_{MPON}	N_{MPOFF}
0b	*77 + MPS_DELTA[6:0]*	215
1b	*7 + MPS_DELTA[6:0]*	255

The default value for MPS_DELTA[6:0] is 4. However the on time can be adjusted by programming the MPS_DELTA bits in the Maintain Power Signature Register (&MPS 0x50):

MPS_DELTA Bit [6:0]	Value
0x01 .. 0x7F	1 .. 127

The Maintain Power timer is enabled by default, but it can be disabled and re−enabled by the MPS_EN bit in the Maintain Power Signature Register (&MPS 0x50):

MPS_EN Bit 7	Meaning
0b	Maintain Power Timer Disable
1b	Maintain Power Timer Enable

The simplest MPS circuit is a power resistor between VPORTP and the MPS pin. For PDs requesting Class 4 or less a 4.32 kΩ 1% MPS resistor should be sufficient to draw at least 10 mA when V_{PSE} = 44 V. For PDs requesting Class 5 or above a 3.09 kΩ 1% MPS resistor should be sufficient to draw at least 16 mA when V_{PSE} = 50 V. While generating the Maintain Power Signature, the power dissipation in the MPS resistor will be significant ($V_{PD}{}^2$ / R_{MPS}) and its package size must be chosen properly.

Autoclass

802.3bt foresees an optional extension of classification known as Autoclass. This allows a 3bt certified PSE to better allocate its power among different PDs.

When the ACS pin is connected to VPORTN, Autoclass is disabled.

When the ACS pin is left floating, Autoclass is enabled and NCL31010 will request an Autoclass measurement to a 3bt type of PSE during classification. If both the ACS bit and the LCF bit in the Classification Result Register (&CRR 0x03) are high, the system must go to the maximum power state according to its assigned Class no later than 1.35 s after power has been applied, and keep the maximum load active until at least 3.65 s after power has been applied. During this period, the PSE will measure the maximum power draw of the PD and allocate this amount of power to the PD.

Table 8. AUTOCLASS

ACS Bit 3	LCF Bit 2	Autoclass Measurement
0b	X	Not requested
1b	0b	
1b	1b	Requested

Peak Power and Transients

Although the PoE standard allows the PD to draw slightly higher peak power during a short time, making use of this is not recommended. It is best to keep this additional margin only to be able to withstand voltage transients on the PSE side. The required recovery time for transients also limits the amount of the port capacitance that can be used.

Under Voltage Lockout

If the port voltage falls below the UVLO_L threshold and remains low for a sufficient amount of time, NCL31010 will enter the poweroff state and turn off the pass−switch.

Once the port voltage falls below the reset threshold V_{rst}, the NCL31010 will re−enter the idle state and can again be detected as a PD requesting power.

Operational Current Protection

In the normal operation mode, NCL31010 will monitor the current through the pass switch and provide protection against soft and hard shorts.

Soft shorts are detected if the current is above the short circuit threshold I_{OC} (6.0 A typ) and a time out delay of 960 μs is passed. After this time−out delay the pass switch is disabled.

A hard short is detected if the voltage across the pass−switch and sense resistor is above V_{OC} (1.2 V typ). The pass gate is switched off within 18 μs in this case.

Once an overcurrent condition is detected during the normal operation mode, the NCL31010 will transition to the offline state and remain there until the port voltage falls below the reset threshold V_{rst}.

Thermal Shutdown

The NCL31010 includes a thermal shutdown which protects the device in the case that the junction temperature is too high. An on−chip sensor monitors the temperature. Once the thermal shutdown threshold (TSD_PoE) is exceeded, all functions are disabled and the device goes into the offline state.

The device will remain in offline until the junction temperature drops and the port voltage falls below the reset threshold V_{rst}.

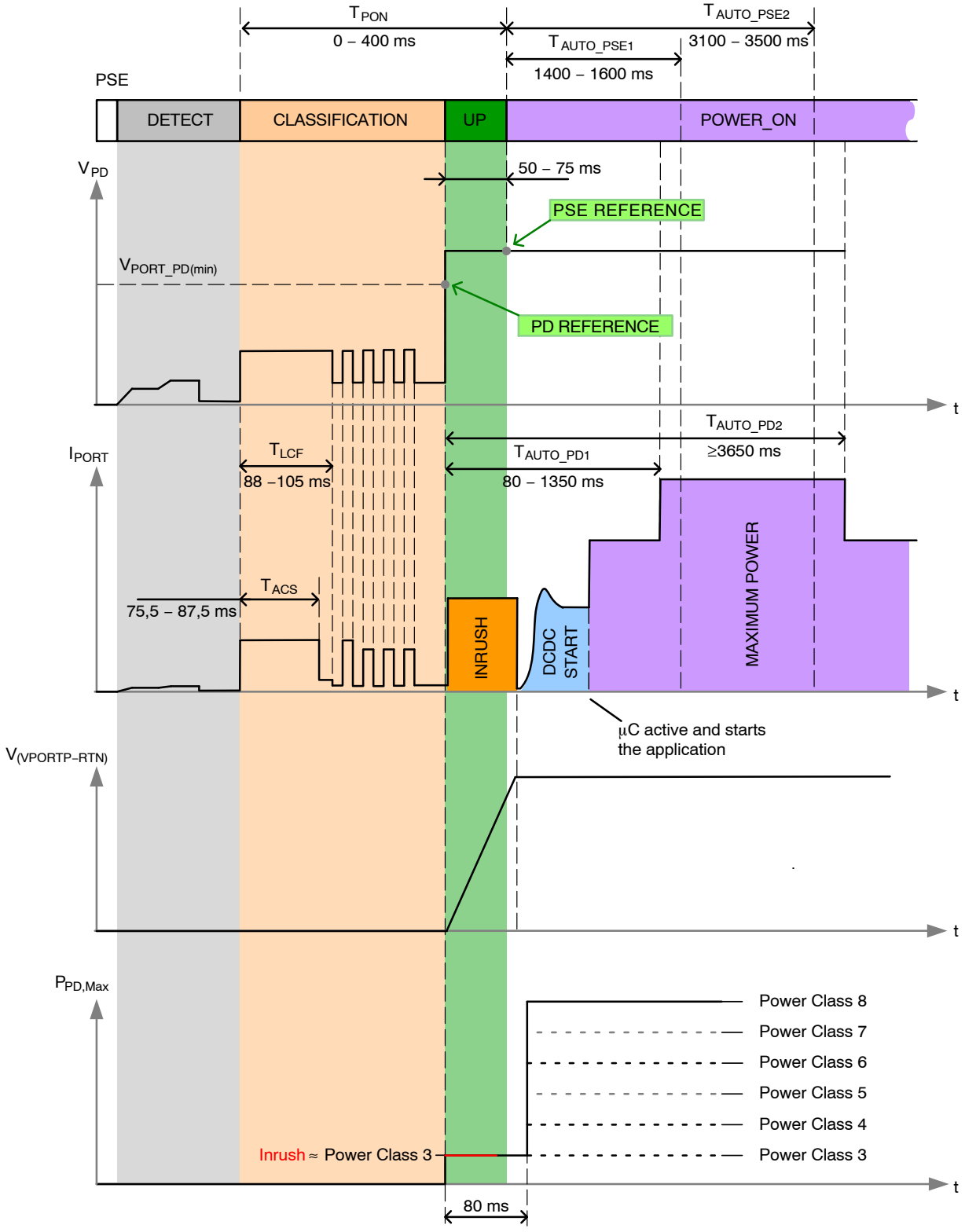


Figure 6. Complete Start−up Diagram of a Class 8 PD with Autoclass

PoE System Overview

The overall PoE standard distinguishes between four Types of PSEs and four Types of PDs.

- Type 1 PSEs and PDs behave according to 802.3af/at
- Type 2 PSEs and PDs behave according to 802.3at
- Type 3 and 4 PSEs and PDs behave according to 802.3bt

Table 9 gives an overview of the system parameters that are allowed and required for operation at a certain power level (assigned Class).

An important parameter is the cable DC resistance (determined by cable type and length).

In general a Cat 5 cable is required when using a Type 3 or Type 4 PD or PSE in the system or when both PSE and PD are of Type 2.

Operation over 4−pair is reserved for Type 3 and 4 PSEs.

PoE Reference

All information regarding Power over Ethernet over 4 Pairs can be found in document IEEE 802.3bt™−2018 which is an amendment to IEEE Std 802.3™−2018.

Table 9. SYSTEM PARAMETERS OVERVIEW

Assigned Class	PSE Type	Minimum Cabling Type	Number of Powered Pairs	PD Type	Requested Class	Standard
1	1	Cat 3 (*) (Note 17)	2p	1	1	802.3af/at
	2	Cat 3				
	3, 4	Cat 3	2p/4p	3		802.3bt
2	1, 2	Cat 3	2p	1	2	802.3af/at
	3	Cat 5 (*) (Note 18)	2p/4p	3		802.3bt
	4	Cat 5				
3	1	Cat 3	2p	1	0,3	802.3af
	1	Cat 3 (*) (Note 19)	2p	1	0,3	802.3at
				2	4	
	2	Cat 3		1	0,3	802.3af/at
				2	4	802.3at
	3, 4	Cat 5	2p/4p	3	3,4/5/6	802.3bt
				4	7/8	
4	2	Cat 5	2p	2	4	802.3at
	3, 4		2p/4p	3	4/5/6	802.3bt
				4	7/8	
5	3, 4	Cat 5	4p	3	5	802.3bt
6	3, 4	Cat 5	4p	3	6	802.3bt
				4	7,8	
7	4	Cat 5	4p	4	7	802.3bt
8	4	Cat 5	4p	4	8	802.3bt

*Critical for:
17. 44 V / 4 W source connected to 3.84 W load over 20 Ω
18. 50 V / 6.7 W source connected to 6.49 W load over 12.5 Ω
19. 44 V / 15.4 W source connected to 13 W load over 20 Ω

DUAL STEP−DOWN CONVERTER FUNCTIONAL DESCRIPTION

The NCL31010 incorporates a dual synchronous step−down switching converter for generating two voltage rails. The top mosfets are internal in NCL31010, whereas the bottom mosfets need to be added externally.

The regulators employ a constant−frequency peak current−mode control scheme with internal compensation. The inductor current is sensed trough a resistance in series with the inductor. This also allows the NCL31010 to measure the average output current (see Metrology section). Depending on the load current, the converter operates in Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM).

The VDD regulator, which is automatically enabled by the PGOOD signal from the PoE block, generates a 3.3 V output voltage with 150 mA output current capability to power the system microcontroller (next to some internal logic on VDDD).

The VDD2 regulator needs to be enabled through the digital interface. The default output voltage of VDD2 is 5 V (with 510 mA output current capability), but other output voltages (and corresponding other output current capabilities) can be programmed by the digital interface: 2.5 V, 3.3 V, 7.2 V, 10 V, 12 V, 15 V or 24 V.

Bottom Mosfet

The bottom mosfets should have the appropriate drain−source on−resistance and voltage rating (≥80 V) while maintaining low output capacitance, low gate charge and good drain−source diode characteristics (reverse recovery). Preferably, the package(s) should be very small to enable a compact PCB layout as well.

Based on above considerations, it is obvious that dual n−channel mosfet FDC8602 seems to be − by far − the best choice to complement NCL31010.

Table 10. DUAL N−CHANNEL MOSFET

Product	V_{DS} (V)	$r_{DS(on)}$ (mΩ)	Package Type
FDC8602	100	350	TSOT−23−6

Switching Frequency

The switching frequency of the NCL31010 DC/DC regulators is 133.3 kHz. This switching frequency is derived from the internal accurate 8 MHz master clock which is divided by 60.

In terms of efficiency and EMI, this low switching frequency is beneficial and yet it allows a small overall solution size (small external inductors and capacitors).

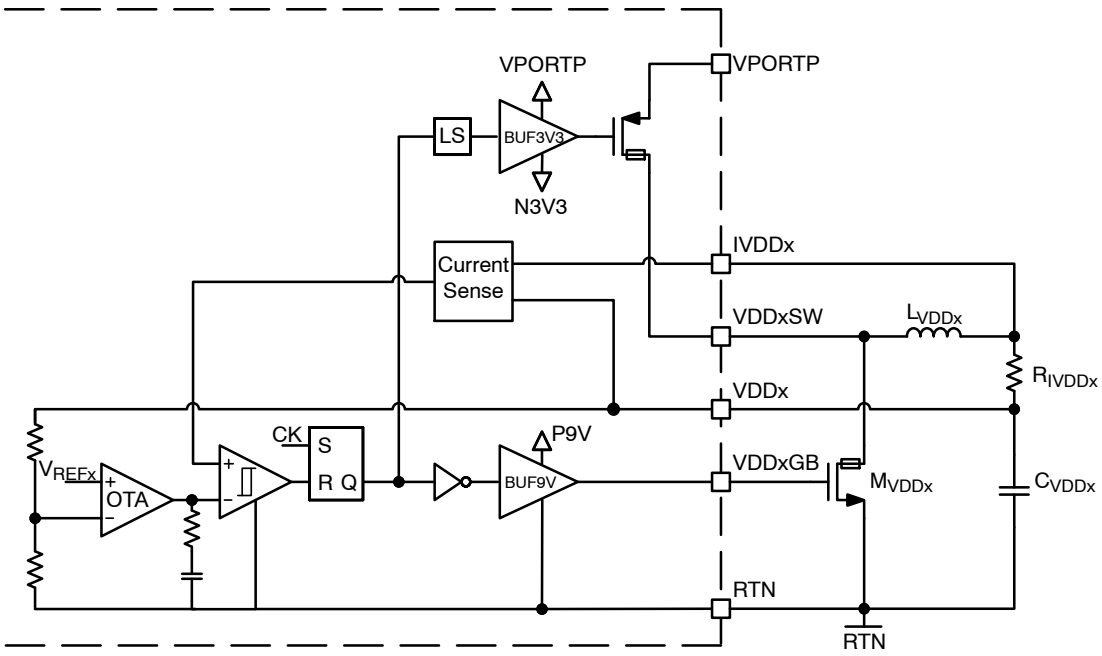


Figure 7. DCDC Block Diagram

Current Sense Resistor and Peak Current Limit

The inductor current is sensed by a current sense resistor in series with the inductor. The sense resistor value configures the gain of the sensed current signal that is compared to the control voltage to determine when the top mosfet needs to be switched off to maintain regulation. The sense resistor value also configures the peak inductor current limit at which the top mosfet will be switched off – despite a higher control voltage – in order to protect the power stage of the converter against overcurrents.

For the VDD regulator, a 750 mΩ sense resistor is recommended.

For the VDD2 regulator with 5 V output voltage, a 200 mΩ sense resistor is recommended. For the other output voltages, the recommended sense resistor value can be found in table 14.

The current sense resistors should have a 1% tolerance.

Inductor

The inductor saturation current should be higher than the maximum peak switch current of the converter. Within an inductor series, smaller inductance values have a higher saturation current rating. Allowing a larger than typically recommended inductor ripple current enables the use of a physically smaller inductor.

For the VDD regulator, a Würth WE−PD Size 7345 Inductor with 390 μH Inductance is recommended.

Table 11. INDUCTOR FOR VDD

Product	L (μH)	$R_{DC\ typ.|max.}$ (Ω)	$I_{SAT\ typ.}$ (A)
744777239	390 ±20%	1.25 | 2.85	0.42

For the VDD2 regulator with 5 V output voltage, the Würth WE−PD Size 1050 P Inductor with 100 μH Inductance is recommended. For the other output voltages, the recommended inductance value from the same inductor series can be found in table 14.

Table 12. INDUCTORS FOR VDD2

Product	L (μH)	$R_{DC\ typ.|max.}$ (mΩ)	$I_{SAT\ typ.}$ (A)
7447714101	100 ±20%	165 | 198	1.8
7447714331	330 ±20%	655 | 750	1
7447714471	470 ±20%	960 | 1100	0.82

Maximum Output Current

The maximum load current that will be available is the peak inductor current limit minus half the peak−to−peak inductor ripple current:

$$I_{OUT} = I_{LIM} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times V_{IN} \times f_{SW}} \quad \text{(eq. 2)}$$

To determine the maximum guaranteed output current above equation should be evaluated with the minimum value of the peak inductor current limit I_{LIM}, of the inductance L (tolerance and saturation) and of the switching frequency f_{sw}. For both the VDD regulator and all output voltages of the VDD2 regulator, conversely, the maximum value of the input voltage V_{IN} (i.e. 57 V) should be used here. Likewise for the output voltage V_{OUT} in above equation an equivalent value $V_{OUT,eq}$ can be used here to incorporate the slight increase in duty cycle with the output current due to the (maximum) resistance of the (bottom) mosfet, the inductor and the sense resistor:

$$V_{OUT,eq}(I_{OUT}) = V_{OUT,typ} + (r_{DS(on)} + R_{DC} + R_{CS}) \times I_{OUT} \quad \text{(eq. 3)}$$

Based on above considerations, the output current capability of both converters operated with the recommended current sense resistance, inductor and bottom mosfet is given below in table 13 and table 14.

Table 13. VDD CONFIGURATION

V_{OUT} (V)	I_{OUT} (mA)	R_{CS} (mΩ)	L (μH)
3.3	150	750	390

Table 14. VDD2 CONFIGURATION

V_{OUT} (V)	I_{OUT} (mA)	R_{CS} (mΩ)	L (μH)
2.5	560	220	100
3.3	515		
5	510	200	
7.2	415		330
10	335	330	330
12	315		
15	285		
24	230	390	470

The listed output current capability still contains some headroom for a temporarily higher output current after a load step−up transient (in order not to influence the load transient response settling time) and for the variation of the switching frequency due to spread spectrum modulation.

Output Capacitor Selection

The VDD and VDD2 regulators do not require any series resistance (ESR) in the output capacitor. Therefore ceramic capacitors with X5R or X7R dielectric are recommended. Unfortunately for these capacitors it is usually not sufficient to only look at the nominal capacitance value: one should always check the Capacitance versus Bias Voltage chart to know the actual remaining capacitance with the output voltage applied!

Some recommended capacitors from the Kemet SMD X5R and X7R series are listed in table 15 (Size 1206) and table 16 (Size 1210).

Table 15. X5R CAPACITORS SIZE 1206

Product	C_0 (µF)	V_{Rated} (V)	C_{VDD2} (µF @ V)
C1206C226K9PAC C1206C226M9PAC	22 ±10% 22 ±20%	6.3	20.3 @ 2.5
			19 @ 3.3
			14.1 @ 5.0
C1206C106K4PAC	10 ±10%	16	9.9 @ 2.5
			9.8 @ 3.3
			9.5 @ 5.0
			9 @ 7.2
			8 @ 10
			6.7 @ 12
C1206C106K3PAC	10 ±10%	25	5.3 @ 15
C1206C475K5PAC	4.7 ±10%	50	3.1 @ 24

Table 16. X5R AND X7R CAPACITORS SIZE 1210

Product	C_0 (µF)	V_{Rated} (V)	C_{VDD2} (µF @ V)
C1210C107M9PAC	100 ±20%	6.3	79.8 @ 2.5
			60.7 @ 3.3
C1210C476M9PAC	47 ±20%	6.3	42.2 @ 5.0
C1210C226K8PAC	22 ±10%	10	17.1 @ 7.2
C1210C106K4PAC	10 ±10%	16	8 @ 10
C1210C106K3RAC	10 ±10%	25	6.7 @ 15
C1210C106M6PAC	10 ±20%	35	9.1 @ 10
			8.7 @ 12
			8 @ 15
			5 @ 24

For X5R and X7R dielectric capacitors the change in capacitance over their operating temperature range is limited to ±15%.

The output capacitor is needed to stabilize the control loop. The gain crossover frequency of the complex open loop gain can be estimated by:

$$f_{gc} \approx \frac{1}{2 \times \pi \times ACR_p \times C_{VDDx}} \quad \text{(eq. 4)}$$

This gain crossover frequency should be significantly lower than half the switching frequency. This places a constraint on the minimum output capacitance value.

The recommended output capacitors for the VDD regulator are listed in Table 17.

Table 17. CAPACITOR(S) FOR VDD

V_{OUT} (V)	C_{VDD} Component(s)	C_{VDD} (µF)
3.3	**22 µF / 6.3 V / 1206**	19
	2 x 10 µF / 16 V / 1206	19.6

The minimum output capacitor values for the VDD2 regulator are listed in Table 18 and those listed in bold are recommended.

Table 18. CAPACITOR(S) FOR VDD2

V_{OUT} (V)	C_{VDD} Component(s)	C_{VDD2} (µF)
2.5	100µF / 6.3V / 1210	79.8
	100 µF / 6.3 V / 1210 + 22 µF / 6.3 V / 1206	100.1
3.3	100 µF / 6.3 V / 1210	60.7
	100 µF / 6.3 V / 1210 + 22 µF / 6.3 V / 1206	79.7
5	47 µF / 6.3 V/ 1210	42.2
	47 µF / 6.3 V / 1210 + 10 µF / 16 V / 1206	51.7
	47 µF / 6.3 V / 1210 + 22 µF / 6.3 V / 1206	56.3
7.2	22 µF / 10 V / 1210	17.1
	2 x 10 µF / 16 V / 1206	18
	22 µF / 10 V / 1210 + 10 µF / 16 V / 1206	26.1
	3 x 10 µF / 16 V / 1206	27
10	10 µF / 35 V / 1210	9.1
	2 x 10 µF / 16 V / 1206	16
12	10 µF / 35 V / 1210	8.7
	2 x 10 µF / 16 V / 1206	13.4
15	10 µF / 35 V / 1210	8
	2 x 10 µF / 25 V / 1206	10.6
	2 x 10 µF / 25 V / 1210	13.4
	3 x 10 µF / 25 V / 1206	15.9
24	10 µF / 35 V / 1210	5
	2 x 4.7 µF / 50 V / 1206	6.2

Transient Response

A first order equivalent circuit of the output impedance of the NCL31010 DC/DC regulators operating in CCM is shown in figure 8.

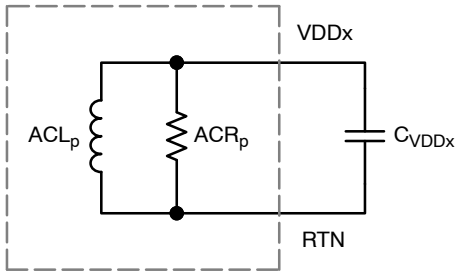


Figure 8. Model for Loop Response

The output capacitor delivers the initial current for transient loads. The output voltage undershoot/overshoot after a load step up/down transient can be estimated by:

$$\Delta v_{VDDx} = - ACR_p \times \Delta i_{VDDx} \quad \text{(eq. 5)}$$

On the other hand, the model explains there is a constraint on the maximum output capacitance value. This can be expressed by the damping factor of the parallel RLC circuit:

$$\xi = \frac{1}{2 \times ACR_p} \times \sqrt{\frac{ACL_p}{C_{VDDx}}} \quad \text{(eq. 6)}$$

It is best to keep the damping factor at or above unity. That it is equivalent to keeping the gain crossover frequency at least 4 times higher than the compensation network zero:

$$f_z = \frac{ACR_p}{2 \times \pi \times ACL_p} \quad \text{(eq. 7)}$$

Otherwise the load step response will become oscillatory.

Input Voltage Range

The minimum input voltage is determined by the NCL31010 VPORTP undervoltage lockout (UVLO). However both the VDD and the VDD2 regulators shall continue to operate without interruption in the presence of transients lasting less than 250 μs at the PSE PI according to IEEE Std 802.3.

Eventually another constraint on the minimum input voltage is related to the subharmonic oscillation phenomenon that might occur in current−mode controlled converters. A rule of thumb is to operate a peak current−mode controller without compensation ramp in CCM up to 33.5% duty cycle in order to keep the Q_p of the current−mode double pole up to 1.932 ($\xi_p \geq 0.259$). For a peak current−mode controller with compensation ramp in CCM, this rule of thumb for the duty cycle becomes:

$$D \leq \frac{0.335}{\left(1 - \frac{L \times S_X}{V_{OUT}}\right)} \quad \text{(eq. 8)}$$

This duty cycle requirement in CCM can be translated into a minimum input voltage requirement:

$$V_{IN} \geq 2.985 \times (V_{OUT} - L \times S_X) \quad \text{(eq. 9)}$$

Obviously without compensation ramp this equation simplifies to:

$$V_{IN} \geq 2.985 \times V_{OUT} \quad \text{(eq. 10)}$$

Above constraint explains why a compensation ramp is implemented on the VDD2 regulator for the 15 V and 24 V output voltage settings. Likewise it explains why there is no need for a compensation ramp on the VDD regulator and on the VDD2 regulator for the other output voltage settings.

The maximum input voltage is determined by the maximum recommended operating voltage of the VPORTP pins (i.e. 57 V).

Input Capacitor

The VPORTP pin 41 must be decoupled to the source of the bottom mosfets (FDC8602) with a ceramic capacitor. The Kemet X7R Size 1210 Capacitor with 1 μF nominal capacitance value is a good option, since the capacitance change over DC bias voltage remains moderate.

Table 19. X7R CAPACITOR SIZE 1210

Product	C_0 (μF)	V_{Rated} (V)	C_{VPORTP} (nF @ V)
C1210C105K1RAC	1 ±10%	100	865 @ 41.1
			800 @ 50
			702 @ 57

Light Load Operation

In Discontinuous Conduction Mode (DCM), the square of the top mosfet on−time is proportional to the output current. When the load becomes lower than the output current corresponding with the minimum on−time, the converter will exhibit pulse skipping behavior.

VDD2 Output voltage

The VDD2 output voltage is programmed in the VDD2_SEL[2:0] bits of Test Register 10 (&TREG10 0x6E):

Table 20.

Bit [2:0]	VDD2 Output Voltage (V)
000b	2.5
001b	10
010b	5
011b	15
100b	3.3
101b	12
110b	7.2
111b	24

The default output voltage of VDD2 is 5 V.

Do NOT write to Test Register 10 when the VDD2 regulator is already enabled.

VDD2 Enable and Shutdown

The VDD2 regulator is enabled when the VDD2_EN bit in the Control Register (&CTRL 0x04) is set.

Table 21.

Bit 0	VDD2EN
0b	Disable VDD2
1b	Enable VDD2

Soft−Start

Both regulators have soft−start implemented in order to limit the overshoot during start−up.

Short Circuit Protection

Besides the peak current limit, the NCL31010 contains additional short circuit protection. If the voltage drops significantly below the regulated value during around 15 ms, that specific converter will be shut down. The converter will be automatically restarted after a cool down period of around 120 ms.

Severe Faults

The NCL31010 monitors the drain−source voltage of a mosfet that is turned−on: if the voltage becomes too large due to excessive current flow through the mosfet, the respective converter will be latched off.

If this occurs on the VDD2 regulator, the VDD2NOK bit in the Status Positive Register (&STATP 0x07) will be set. This will generate an interrupt on the INTB pin if the VDD2NOK bit in the Interrupt Positive Mask Register (&INTP 0x0B) was not masked.

LED DRIVER FUNCTIONAL DESCRIPTION

The NCL31010 incorporates a peak current−mode buck LED controller. The controller operates only in CCM mode and is designed to drive high power LED loads up to 90 W and beyond. A block diagram of the concept with the essential parts is given in figure 9.

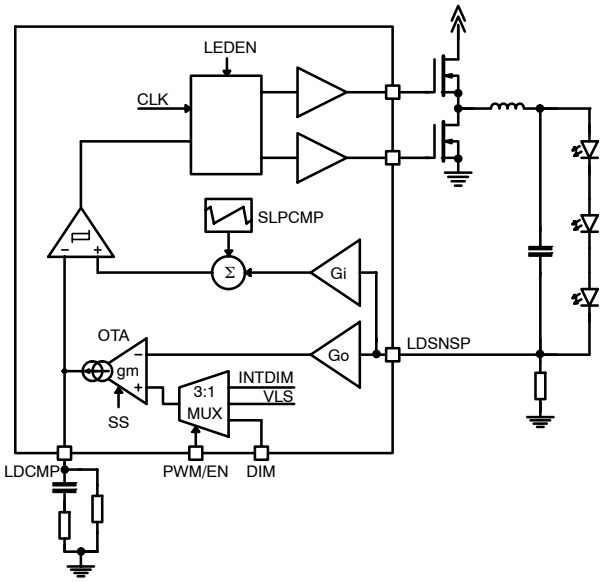


Figure 9. LED Driver Block Diagram

The LED driver is enabled when the LEDEN bit in the CTRL register is set. When the LED driver is enabled it is switching and regulates a current controlled by the DIMCTRL voltage shown in figure 9. The relationship between DIMCTRL and the LED current is given below.

$$I_{LED} = \frac{(VDIMCTRL - V_{CSA\_0})}{R_{SNS} \times 7.333} \quad \text{(eq. 11)}$$

Several sources can be multiplexed to the DIMCTRL signal, see figure 10.

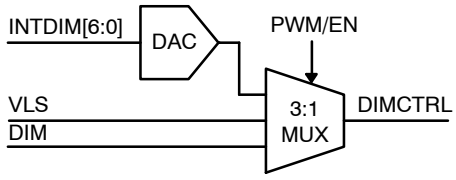


Figure 10. DIM Selection

The analog DIM input gives the best dimming performance in terms of linearity, bandwidth and accuracy.

The DIM pin threshold voltage that provides exactly zero current is the VCSA_0 voltage. Applying a voltage below the VCSA_0 lower limit guarantees zero current.

The PWM pin can be used for PWM dimming. A PWM signal on the PWM input can be used to switch the LED current between zero and the level defined by the voltage level on the DIM pin. The duty−cycle of this signal will define the average LED current. To have a good linear relationship between the duty−cycle and the LED current the frequency of this signal must be below 1 − 2 kHz. This method provides a simple way to use PWM directly to control the LED current, however it does not give the best dimming accuracy and linearity and the duty−cycle range is limited. When the PWM digital input pin is low, the MUX connects VLS to DIMCTRL. VLS has a steady value just below VCSA_0 to guarantee that the LED driver is regulating zero current when PWM = 0. When the PWM pin is high, the voltage on the DIM pin is connected to DIMCTRL.

When the INTDIMEN bit in the INTDIM register is set the internal 7−bit DAC output is connected to DIMCTRL. In this case, the LED current will depend on the value programmed in the 7 bits of the INTDIM register. The relationship between the register value and the DAC output voltage is given below.

$$V_{INTDIM} = \frac{V_{REF} \times (INTDIM[6:0] + 1)}{128} \quad \text{(eq. 12)}$$

The internal DAC can be useful when, for example, the host MCU is being re−flashed and the DIM voltage is not controlled during this period. In this case the MCU can instruct the internal DAC to take control of DIMCTRL net moments before the MCU firmware is under maintenance. This is called ‘Warm Boot’.

Voltage Reference

The NCL31010 provides a precise (±0.3%) 2.4 V reference voltage on the VREF pin, which can be used by external components, for example, as the reference of an external PWM to DIM circuit or a DAC that controls the DIM pin voltage. The load on this pin must be limited to 2 mA to ensure the accuracy of the voltage. The advantage of using this VREF is that the VREF voltage and the VCSA_0 voltage (the threshold point for zero current) are related. If VREF deviates, VCSA_0 will deviate in the same direction by a proportional factor, thus the LED current regulation inaccuracy of a circuit that is VREF based does not suffer from the VREF deviation.

Sense Resistor

Select an appropriate sense resistor based on the maximum LED current. The resistor value can be calculated according to:

$$R_S = \frac{(VREF - VCSA\_0)}{7.333 \times Iled_{max}} \quad \text{(eq. 13)}$$

Make sure to select a sense resistor that has a value between 50 mΩ and 300 mΩ. Consider the power rating and the accuracy. A 1 W or 2 W / 1% sense resistor is sufficient for most applications.

Buck Inductor

The rule of thumb is to choose the inductor so that the peak−peak current ripple in the inductor is 20..30% of the max dc−current. Calculate the required inductance according to:

$$L = \frac{Vi}{4 \times fs \times Iled_{max} \times 0.3} \quad \text{(eq. 14)}$$

Make sure that the specified RMS current rating of the inductor (typically the current that results in a temperature increase of 40°C due to copper losses) is at or above the max dc−current used in the application. The saturation current rating minus 20% derating should still be at or above the largest peak current. Use the formulas below to find appropriate minimum RMS current and saturation current values.

$$Irms > Iled_{max} \quad \text{(eq. 15)}$$

$$Ir_{max-pkpk} = \frac{Vi_{max}}{4 \times fs \times L} \quad \text{(eq. 16)}$$

$$Isat > \left(Iledmax + \frac{Ir_{max-pkpk}}{2} \right) \times 1.2 \quad \text{(eq. 17)}$$

Output Capacitor

The purpose of the output capacitor is to filter the high frequency inductor ripple current to some extent. This must be a 100 V rated ceramic capacitor(s) with low ESR. The required output capacitor depends on the switching frequency, the expected LED ripple current ($Ir_{LED-pkpk}$), the dynamic resistance of the LED string (Rd) and the inductor ripple current ($Ir_{max-pkpk}$). The expression is given below:

$$C_O = \frac{8}{\pi^2} \times \frac{Ir_{max-pkpk}}{2\pi \times fs \times Ir_{LED} \times Rd} \quad \text{(eq. 18)}$$

Substituting Ir_{max} gives:

$$C_O = \frac{Vi_{max}}{31 \times fs^2 \times L \times Ir_{LED-pkpk} \times Rd} \quad \text{(eq. 19)}$$

A reasonable output capacitor value would be anything between 100 nF and 1 − 3 μF. Try to avoid 1608 (metric) packages or smaller to avoid audible noise. The output capacitance has no significant effect on stability.

Bandwidth & Stability

The control loop in this configuration exhibits no poles to be compensated in the bandwidth area so a single compensation capacitor connected to LDCMP pin will suffice. This strategy is suitable for a bandwidth up to $1/10^{th}$ of the switching frequency and provides a phase margin of 60 − 75 degrees. The compensation capacitor can be calculated as:

$$C_C = 2.44 \times \frac{G_M}{2 \times \pi \times f_C} \quad \text{(eq. 20)}$$

f_C is the wanted cross−over frequency and G_M = 1 mS.

Slope Compensation

Since a peak−current−mode buck convertor is sensitive to sub−harmonic oscillations for duty−cycles above 33% slope compensation must be added. There is a minimum amount of slope needed to damp sub−harmonic oscillations within one switching cycle. The slope value can be programmed in the SLPCMP register. The default value is a good setting for most applications and normally no changes have to be made to this register. If the phase margin is not sufficient (<60 degrees), program '0' to SLP1 and SLP2 field in the SLPCMP register.

The required amount of slope increases with output voltage and the ratio from output to input voltage (duty−cycle). A separate slope setting can be programmed for slopes below 50% duty−cycle (SLP1 field) and above (SLP2 field). The possibilities for SLP1 and SLP2 fields are presented in table 22 and 23 respectively. The default value for SLP1 and SLP2 is set to 0.1 V/μs and 0.3 V/μs. Increase SLP1 one level if sub−harmonic oscillation is seen below 50% duty−cycle. Increase SLP2 one level if subharmonic oscillation is seen above 50% duty−cycle.

Table 22. SLP1 VALUES

SPL1 Register Value	Slope [V/μs]
0	0.1
1	0.2
2	0.3
3	0.4

Table 23. SLP2 VALUES

SPL2 Register Value	Slope [V/μs]
0	0.3
1	0.4
2	0.6
3	0.9

Switching Frequency

All the clocks in the chip are derived from a main 8 MHz clock. The LED driver's switching frequency can be programmed with the LEDFC register. The value in the register relates to the LED driver switching frequency clock according to table 24. The default switching frequency is 500 kHz. For most applications that regulate LED currents below 1.5 A, a switching frequency of 500 kHz is a good choice. For applications that regulate above 1.5 A, 400 kHz is recommended.

Table 24. SWITCHING FREQUENCY

LEDFC [5:0]	DIVISOR	LED_CLK [kHz]
0	8	1000.00
1	10	800.00
2	12	666.67
3	14	571.43
4	16	500.00
5	18	444.44
6	20	400.00
7	22	363.64
8	24	333.33
9	26	307.69
10	28	285.71
11	32	250.00
12	34	235.29
13	38	210.53
14	42	190.48
15	46	173.91
16	52	153.85
17	56	142.86
18	64	125.00
19	70	114.29
20	76	105.26
21	84	95.24
22	102	78.43
23	112	71.43
24	124	64.52
25	150	53.33
26	180	44.44

Switching Transistors

The selection of the switching transistors is a critical aspect for the correct functioning of the LED driver. It can significantly impact the power efficiency and thermal performance. The top fet in particular will dissipate most of the switching losses. Because this component is essential to the LED driver performance it is advised to select one of the validated transistors for top and bottom given in table 25. The transistors are ranked high−low for efficiency. The typical LED driver efficiency achievable with the proposed transistors for 30 − 70 W range is 97%. The best combination is to use FDMA037N08L as bottom fet and NVTFS6H880N or NVTFS6H888N as top fet.

Table 25. TRANSISTOR SELECTION

	Product	V_{DS} (V)	$r_{DS(on)}$ (mΩ)
Top	NVTFS6H880N	80	32
	NVTFS6H888N	80	55
	NVTFS6H860N	80	21.1
Bottom	FDMA037N08LC	80	36.5

Do not use external gate resistors for the transistors. The chip uses the voltages at the gate nodes as feedback for desaturation protection and fast switching.

Thermal Considerations

Additional copper is needed for good thermal performance. A typical design with LED currents below 2 A (<60 W) requires a small (both copper sides) cooling plane with size 2 − 3 cm^2 connected to the drain of the top fet. For 2 A and above (>60 W), a 3 − 4 cm^2 copper plane is recommended on both sides. The bottom fet drain connection should also have a small 0.5 − 1 cm^2 copper plane.

Metrology

The NCL31010 incorporates a high accuracy metrology block that measures several voltages, currents and temperatures in the system. This is made possible by an internal 10−bit ADC, which is multiplexed to measure VPORTP, VDD1, VDD2, VLED, ILED, IPORTP, IVDD, IVDD2 and TLED. The metrology measurements can be enabled with the DIAG_EN bit in the CTRL register. The measurements are referenced to RTN and are sampled every 249 ms. The measurements can be read out from the 16−bit registers. The relationship between the measured voltage/current/temperature and the values read in the registers is given in equation 21 to equation 29.

$$VPORT = VPORTP_{reg} \times \frac{5000}{201} \times \frac{VREF}{2^{16}} \quad \text{(eq. 21)}$$

$$IPORT = IPORTP_{reg} \times \frac{VREF}{6 \times Rs \times 2^{16}} \quad \text{(eq. 22)}$$

$$VDD = VDD_{reg} \times \frac{3}{2} \times \frac{VREF}{2^{16}} \quad \text{(eq. 23)}$$

$$VDD2 = VDD2_{reg} \times \frac{32}{3} \times \frac{VREF}{2^{16}} \quad \text{(eq. 24)}$$

$$IDD = IDD_{reg} \times \frac{VREF}{10 \times Rs \times 2^{16}} \quad \text{(eq. 25)}$$

$$IDD2 = IDD2_{reg} \times \frac{VREF}{10 \times Rs \times 2^{16}} \quad \text{(eq. 26)}$$

$$VLED = VLED_{reg} \times \frac{35}{2} \times \frac{VREF}{2^{16}} \quad \text{(eq. 27)}$$

$$ILED = ILED_{reg} \times \frac{3}{22} \times \frac{VREF}{Rs \times 2^{16}} \quad \text{(eq. 28)}$$

$$TLED = TLED_{reg} \times \frac{33}{24} \times \frac{VREF}{2^{16}} \quad \text{(eq. 29)}$$

Status Bits

The NCL31010 has ten status−monitoring bits, spread over two 8−bit registers. The status bits are active when a particular condition is met. As an example, STAT1.TW is active when the internally measured temperature exceeds the temperature limit set by the TWTH (thermal warning threshold). When the condition disappears, the corresponding bit becomes inactive immediately. The actual, immediate, value of the status bits can be accessed through the read−only status registers (STAT). Status bits can become active only very briefly. As such, reading the STAT is not sufficient to detect the activation of a fault in an NCL31010 device: between subsequent reads, the fault could have appeared and disappeared. The read−only ‘Status Positive Transition’ register (STATP) addresses this problem. It reflects all status bits that have become active since the last read of the STATP. Thus, by reading STAT and STATP, the host microcontroller can determine whether a status bit has been active since the last read, and whether it is still active. The STATP bits are cleared on read. The addresses of the STAT and STATP are contiguous. Thus the microcontroller can read out the STAT and STATP atomically, ensuring coherent information is received.

In addition to STATP, the ‘Status negative transition’ STATN register activates when the fault disappears (negative edge STAT register). This register is also cleared on read. The status signals are grouped in two categories: warnings and errors. This is discussed below.

Warnings

Some of the status bits can be considered as a warning signal meaning there is no need for a very fast response from the NCL31010 itself and the decision can be left up to the microcontroller. The NCL31010 takes no action other than signal that a threshold is crossed using the status bits. The status bits that are considered as warnings are: TW, LEDTSD, LEDTW, LEDOV, LEDUV, VDD2OC, VDDOC. These warnings are reflected in the STAT1 and STATP1/STATN1 registers. These analog values are measured by the metrology block with the internal ADC and a sampling rate of 249 ms. For the warnings, all the thresholds and hysteresis values are programmable except for TW. An example for LEDTW is given in figures 11 and 12.

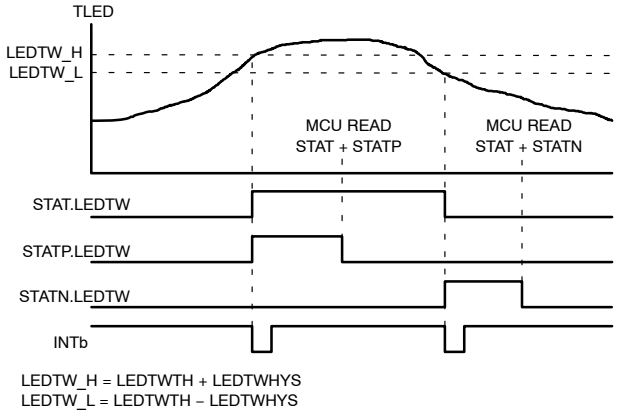


Figure 11. LEDTW [INTCFG=1 INTP/INTN=1]

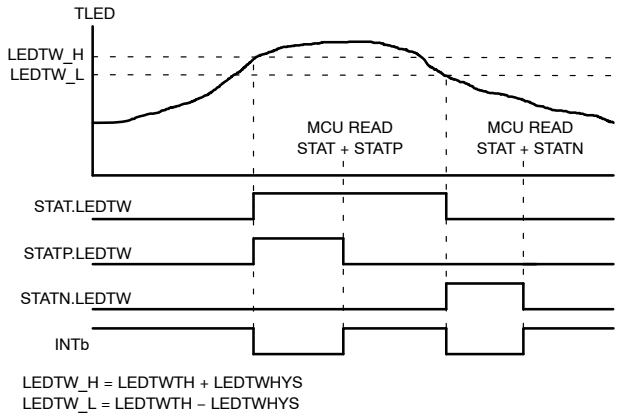


Figure 12. LEDTW [INTCFG=0 INTP/INTN=1]

A warning occurs when a programmable limit is crossed. For example, when the voltage on the TLED pin exceeds the LEDTWTH+LEDTWHYS threshold the status LEDTW bit is set in the STAT register. The threshold and hysteresis are programmable in the LEDTWTH and LEDTWHYS registers. Only when the voltage on the TLED pin drops below LEDTWTH−LEDTWHYS the LEDTW bit in the STAT is cleared. If the LEDTW bit in the Interrupt Mask register is set a pulse interrupt will be given on the INTb pin when the LEDTW bit is set in the STAT. The warnings except TW are disabled when LEDTWTH + LEDTWHYS > 1022. All warnings except TW are disabled by default because they have 1023 in their threshold registers. All the warnings are explained below.

TW: Thermal Warning

The TW bit in the STAT is set if the junction temperature of the NCL31010 goes above TW_H. This warning is active by default and cannot be de−activated. This threshold is not programmable.

LEDTW: LED Thermal Warning

This warning will occur if the voltage on TLED pin is above LEDTWTH+LEDTWHYS. Typically, an NTC is mounted on the LED load and connected to TLED and RTN. This warning is not active by default and the threshold and hysteresis are programmable.

LEDTSD: LED Thermal Shutdown

This warning will occur if the voltage on TLED pin is above LEDTSD + LEDTSDHYS. Typically, an NTC is mounted on the LED load and connected to TLED and RTN. This warning is not active by default and the threshold and hysteresis are programmable.

LEDOV: LED Overvoltage

This warning will typically occur if the LED string is an open circuit. The LEDOV bit in the STAT is set if the VLED pin voltage goes above LEDOVTH + LEDOVHYS. The threshold and hysteresis are programmable.

LEDUV: LED Undervoltage

This warning will typically occur if the LED string is a short circuit. The LEDUV bit is set in the STAT. This warning is not active by default and the threshold and hysteresis are programmable.

VDDOC and VDD2OC: VDDx Overcurrent

A warning is given if the average current is above VDDxOCTH + VDDxOCHYS. Note that the DC−DC's also have a current limiting hick−up mode built−in. This warning is not active by default and the threshold and hysteresis are programmable.

Errors

There are severe error conditions that require NCL31010 to disable the block that triggered the error immediately before any damage can occur. These are LEDNOK, LEDOC and VDD2NOK. These errors are reflected in the STAT2 and STATP2/STATN2 registers. The STAT signals behavior is the same for errors and warnings. Note that typically STATN has no use for errors because the fault is gone when the micro−controller reads the registers.

In case of a desaturation fault during the switching of the transistors in the LED driver a LEDNOK error is triggered and NCL31010 will disable the LED driver block. NCL31010 will remain disabled until the LEDEN bit is reset by the user. Similarly if a desaturation fault occurs in the DC−DC2 block a VDD2NOK error is triggered and the DC−DC2 block is disabled. A LEDOC error is triggered if the LED driver sense resistor voltage crosses the OCP_TH threshold indicating a LED overcurrent. The LED block is disabled and resumes after a reset of the LEDEN bit. See figures 13 and 14 for clarification.

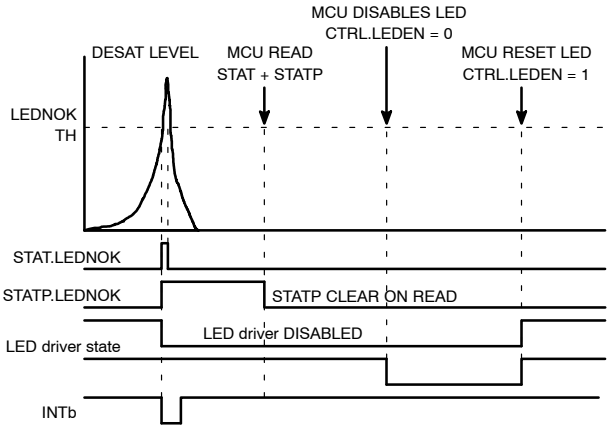


Figure 13. LEDNOK [INTCFG=1 INTP=1 INTN=X]

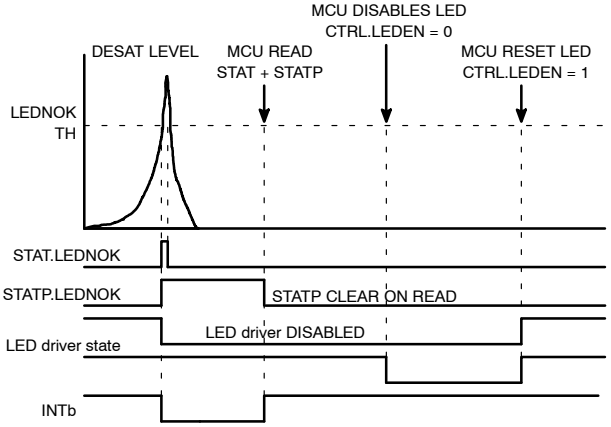


Figure 14. LEDNOK [INTCFG=0 INTP=1 INTN=X]

An error indicates that there is a hardware issue. Further explanation for each of the errors is given below.

TSD: Thermal Shutdown

When the junction temperature of the NCL31010 reaches TSD_H, the NCL31010 will shut down all functions and go into reset state. This includes disconnecting the pass switch. Therefore, the PSE will disconnect the device after the MPS dropout time. The device will remain in reset until the junction temperature drops below TSD_L and a new detection and classification cycle is started by the PSE.

VDD2NOK: Desaturation Error Switching Transistors

NCL31010 will shut−down DC−DC2 if this error occurs. DC−DC2 can be restarted if VDD2EN bit in CTRL is reset.

LEDNOK: Desaturation Error Switching Transistors

NCL31010 will shut−down LED block if this error occurs. The LED block can be restarted if LEDEN bit in CTRL is reset.

LEDOC: LED Overcurrent

This error can occur if the LED load wires are not well connected to the driver board and contact−bounce occurs. A sudden failure of the sense resistor can also trigger this error. NCL31010 will shut−down the LED block if this error occurs and set the LEDOC bit in the STATP.

Interrupts

The NCL31010 has a flexible interrupt mechanism that obviates the need for frequent polling. With an appropriate configuration of the two interrupt mask registers (INTP and INTN), most applications will not require polling at all, while providing for coherent status awareness in the host microcontroller. When an interrupt is triggered, INTb is pulled low. INTb is an open−drain pin to ensure multiple I^2C bus participants can share the same interrupt line. A pull−up resistor must be provided externally. The NCL31010 provides an open−drain, active−low interrupt pin that activates, i.e. pulled low, when any *interrupt condition* is satisfied. An interrupt condition is satisfied if any of the bits in the STATP or STATN register is active and if the corresponding bit in the INTP and INTN are unmasked (= set).

If CTRL.INTCFG is zero (default) level interrupt is used and INTb goes low as long as the interrupt condition is satisfied. If CTRL.INTCFG is set, INTb is configured for pulsed interrupt and INTb will go low for about 10us every time the interrupt condition is satisfied.

Spread Spectrum

The purpose of spread spectrum is to continuously change the clock frequency used by the switching convertors in a periodic pattern to reduce the detected energy levels at a given frequency. It will improve the results of conducted EMI tests, not for radiated EMI. The spread spectrum block modulates the main 8 MHz clock according to a number of discrete steps in a triangular pattern as shown in figure 15. The spread clock signal is used by digital, LED driver and DC−DC convertors. The spread spectrum is disabled by default and can be enabled with the JIT_EN bit in the LEDFC register. The amount of spreading can be configured with the FDEV register. The deviation (%) is the amplitude variation towards the main clock. When the main clock is divided the same amount of spread (%) is still present on the divided clock. Table 26 relates the value for FDEV register to the amount of spreading. The default spreading when spread spectrum is enabled is 3%.

Table 26. FREQUENCY DEVIATION

FDEV [2:0]	Δ (%)
0	3
1	5
2	6
3	8
4	10
5	11
6	12.5
7	14

The FMOD register value affects the modulation period (Tmod) of the triangular signal. The default value for fmod is 400 Hz. The value in the FMOD register relates to fmod according to table 27.

Table 27. MODULATION FREQUENCY

FMOD [1:0]	fmod (1/Tmod)
0	200 Hz
1	400 Hz
2	800 Hz
3	1600 Hz

The spread spectrum is illustrated with figure 15.

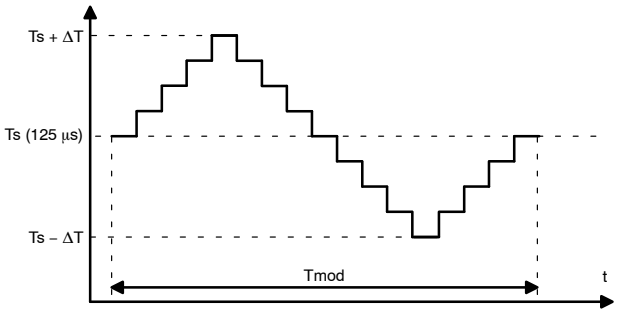


Figure 15. Spread Spectrum

Both fmod and fdev affect the modulation index of the frequency modulated clock signal.

$$MI = \frac{fdev}{fmod} \qquad \text{(eq. 30)}$$

More suppression is achieved when the modulation index is higher. This is true if the RBW of the spectrum analyzer would be infinitely small, instead the RBW is 9 kHz for conducted emission measurements (150 kHz to 30 MHz) and 120 kHz for radiated emission measurements (30 MHz to 1 GHz). When the RBW is 9 kHz the spectrum analyzer will show better suppression if fmod has the maximum value.

Address Selection (NCL31010I)

The NCL31010 comes in two variants. One with SPI interface and one with I^2C interface. This is defined by OTP (One−time programmable memory) in the chip. In case the device is configured as I^2C slave the ADDR1 and ADDR2 pins define the I^2C slave bus address. The device can have 6 possible I^2C slave addresses to differentiate devices on the same I^2C−bus. The mapping between the logic level on these pins and the I^2C slave address is given in table 28.

Table 28. SLAVE ADDRESS

ADDR1_CSB	ADDR2_MISO	Slave Address
RTN	RTN	0x50 (1010000)
VDD	VDD	0x52 (1010010)
FLOAT	RTN	0x54 (1010100)
RTN	VDD	0x56 (1010110)
VDD	RTN	0x58 (1011000)
FLOAT	VDD	0x5A (1011010)

I²C Interface (NCL31010I)

The I²C interface can be used to interface with the NCL31010 in order to read or write its registers. The NCL31010 operates as an I²C slave device. The SDA and SCL lines comply with the I²C electrical specification and should be terminated with external pull−up resistors. The device supports the maximum bus speed of 400 kbit/s.

Figure 16 shows how an I²C write operation is performed. The master gives the Start condition followed by the 7−bit slave address and the read−write bit. The slave acknowledges the address. The master then places the register address on the bus. This is again acknowledged by the slave. Finally the data byte is placed on the bus by the master. The slave must acknowledge this. The master can write more than one byte in one transaction if he wishes. Writing to the registers in this case is contiguous. As more data bytes follow, the register address is auto−incremented.

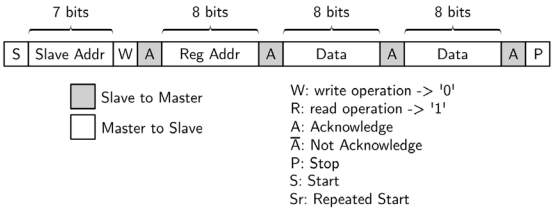


Figure 16. I²C Write Operation (2 bytes)

Figure shows how to perform an I²C read operation. The first part of a read operation is the same as for a write operation. The master provides the slave address, write bit, and register address were to read from. It then provides a repeated start condition which behaves the same as a start condition. It provides the slave address again, but this time it uses it makes the read−write bit zero to indicate a read operation. The slave acknowledges and places the requested data byte on the bus. If the master responds with a NACK (not acknowledge) and a STOP condition the message transaction is terminated. If instead the master uses an ACK it indicates to the slave that it wants to read more bytes. The slave will auto−increment the register address to read from and put the bytes on the bus as shown in Figure 18.

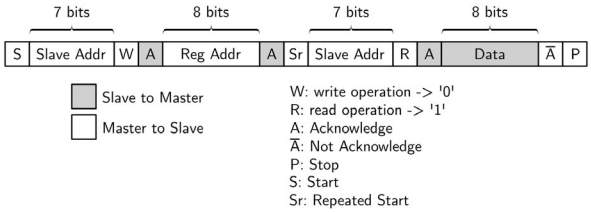


Figure 17. I²C Read Operation (1 byte)

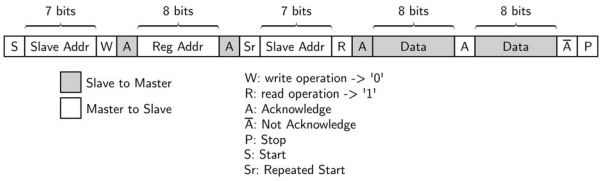


Figure 18. I²C Read Operation (2 bytes or More)

SPI Interface (NCL31010S)

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with NCL31010S. The device acts always as a Slave and cant initiate any transmission. The operation of the device is configured and controlled by means of registers which are observable for read and/or write from the Master. ’

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCL/CLK) synchronizes shifting and sampling of the information on the two serial data lines, MOSI (SDA_MOSI pin) and MISO (ADDR2_MISO pin). The MISO signal is the output from the slave and MOSI is the master output.

NCL31010S is configured for SPI MODE 2. This means that the signal on the MOSI/MISO data lines is sampled on the negative clock edge and that the CLK signal is high when idle. Note that the NCL31010S expects the first data signal to be present and stable on the first negative clock edge.

Figure 19 shows how to perform a SPI write operation. The master pulls the chip select signal low and a little later the master provides a minimum sequence of 16 clock cycles. During the first eight clock cycles, the master provides the register address [A6:A0] and the read−write bit on the MOSI line. If the read−write bit is high, a read operation is selected. During the following eight clock cycles, the slave clocks in the data byte [D7:D0]. If the master provides a multiple of eight clock cycles, more bytes can be written contiguously. The register counter is automatically incremented.

Figure 20 demonstrates a SPI read operation. The same principle applies as with a write operation only now the slave puts the contents of the addressed register on the MISO line during the last eight clock cycles. If the master provides a multiple of eight clock cycles more registers can be read contiguously.

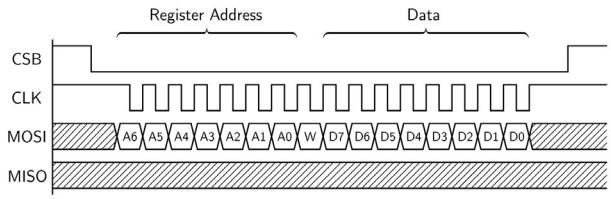


Figure 19. SPI Write Operation (1 byte)

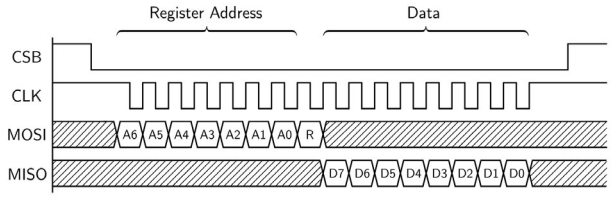


Figure 20. SPI Read Operation (1 byte)

Multiple SPI slaves can be used with one SPI master as shown in figure 21. A separate CSB signal is required for each slave. Daisy chaining is not supported.

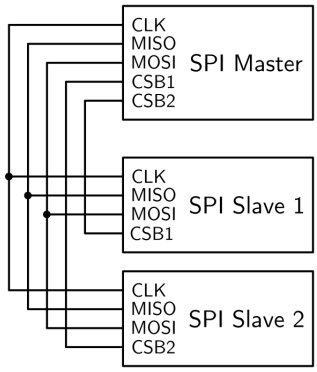


Figure 21. SPI Multi Slave

REGISTER MAP

Table 29. REGISTER MAP

Addr	Name	Reset	Bits	MSB							LSB
00_H	RID1	00_H	7:0	MANUF_H							
01_H	RID2	75_H	7:0	MANUF_L				PART_H			
02_H	RID3	$8C_H$	7:0	PART_L					REV		
03_H	CLASS	00_H	7:0	Rsv.			ACS	LCF	CLASSEVENT		
04_H	CTRL	00_H	7:0	INTCFG	Rsv.				DIAG_EN	LED_EN	VDD2_EN
05_H	STAT1	00_H	7:0	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
06_H	STAT2	00_H	7:0	Rsv.					LEDOC	LEDNOK	VDD2NOK
07_H	STATP1	00_H	7:0	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
08_H	STATP2	00_H	7:0	Rsv.					LEDOC	LEDNOK	VDD2NOK
09_H	STATN1	00_H	7:0	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
$0A_H$	STATN2	00_H	7:0	Rsv.					LEDOC	LEDNOK	VDD2NOK
$0B_H$	INTP1	00_H	7:0	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
$0C_H$	INTP2	00_H	7:0	Rsv.					LEDOC	LEDNOK	VDD2NOK
$0D_H$	INTN1	00_H	7:0	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
$0E_H$	INTN2	00_H	7:0	Rsv.					LEDOC	LEDNOK	VDD2NOK
10_H	VBB	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
12_H	IBB	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
14_H	VDD1	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
16_H	IDD1	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
18_H	VDD2	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
$1A_H$	IDD2	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
$1C_H$	VLED	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
$1E_H$	ILED	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
20_H	TLED	0000_H	15:8	ADCv							
			7:0	ADCv			Rsv.				
22_H	VDD1OCTH	$FFFF_H$	15:8	val							
			7:0	val			Rsv.				
24_H	VDD2OCTH	$FFFF_H$	15:8	val							
			7:0	val			Rsv.				
26_H	TLEDTWTH	$FFFF_H$	15:8	val							
			7:0	val			Rsv.				

Table 29. REGISTER MAP (continued)

Addr	Name	Reset	Bits	MSB							LSB
28_H	TLEDTSDTH	$FFFF_H$	15:8	val							
			7:0	val							
$2A_H$	VLEDOVTH	$FFFF_H$	15:8	val							
			7:0	val							
$2C_H$	VLEDUVTH	$FFFF_H$	15:8	val							
			7:0	val							
30_H	VDD1OCTH_HYS	$0A_H$	7:0	Rsv.	val						
31_H	VDD2OCTH_HYS	$0A_H$	7:0	Rsv.	val						
32_H	TLEDTWTH_HYS	$0A_H$	7:0	Rsv.	val						
33_H	TLEDTSDTH_HYS	$0A_H$	7:0	Rsv.	val						
34_H	VLEDOVTH_HYS	$0A_H$	7:0	Rsv.	val						
35_H	VLEDUVTH_HYS	$0A_H$	7:0	Rsv.	val						
40_H	INTDIM	00_H	7:0	EN	DACv						
41_H	LEDFC	04_H	7:0	JIT_EN	FREQ						
42_H	SLCMP	$0A_H$	7:0	Rsv.					SLP2	SLP1	
50_H	MPS	84_H	7:0	EN	DELTA						
51_H	FDEV	06_H	7:0	Rsv.	SSLUT_DIS		Rsv.		FDEV		
52_H	FMOD	01_H	7:0	Rsv.						val	

REGISTER RID1
Manufacturer, part and revision identification.

	7	6	5	4	3	2	1	0
	MANUF_H							
	r							
	0							

Bits 0–7, MANUF_H: Manufacturer ID.

REGISTER RID2
Manufacturer, part and revision identification.

	7	6	5	4	3	2	1	0
	MANUF_L				PART_H			
	r				r			
	7				5			

Bits 4–7, MANUF_L: Manufacturer ID
Bits 0–3, PART_H: Part ID

REGISTER RID3
Manufacturer, part and revision identification.

	7	6	5	4	3	2	1	0
	PART_L					REV		
	r					r		
	11_H					4		

Bits 3–7, PART_L: Part ID.
Bits 0–2, REV: Revision ID.
1: N1A
2: O1A
3: P1A
4: Q1A

REGISTER CLASS
PoE classification Register

	7	6	5	4	3	2	1	0
	Rsv.				ACS	LCF	CLASSEVENT	
	r				r	r	r	
	0				0	0	0	

Bits 4–7: Reserved, do not use.
Bit 3, ACS: Indicates whether the PD has signaled the PSE that it wants to use auto−classification.
0: The PD will not attempt to use auto−classification.
1: The PD has signaled the PD that it might want to use auto−classification.
Bit 2, LCF: Indicates whether a Long Class Finger is detected.
0: No LCF given by PSE. A standard MPS pulse is given if MPS enabled.
1: LCF given by PSE. A MPS pulse with longer period is given if MPS enabled.
Bits 0–1, CLASSEVENT: These bits indicate the assigned power class by the PSE. The PD should always keep the power consumption below this power class budget.
If the requested power budget using the class resistors on the board is lower than the power class budget, the PD should limit the power budget to whichever is lower.
0: Lowest power class, 13 W.
1: Power class, 25.5 W.
2: Power class, 51 W.
3: Power class, 71 W.

REGISTER CTRL
Control register for the major blocks in the system.

	7	6	5	4	3	2	1	0
	INTCFG	Rsv.				DIAG_EN	LED_EN	VDD2_EN
	r/w	r				r/w	r/w	r/w
	0	0				0	0	0

Bit 7, INTCFG: Define how the interrupt on the INTB line behaves.
0: The INTB pin is pulled low when a interrupt occurs. It stays low until the STATPx registers are read and provided the alert condition is gone (STATx register bits are cleared).
1: A pulse is given on each interrupt by the INTB pin.
Bits 3–6: Reserved, do not use.
Bit 2, DIAG_EN: The diagnostics function measures voltages, currents and temperatures in the system using the internal ADC.
0: Diagnostics block is disabled.
1: Diagnostics block is enabled.

Bit 1, LED_EN: Enable bit for the LED driver.
0: LED driver is disabled.
1: LED driver is enabled.
Bit 0, VDD2_EN: Enable bit for DC/DC2 converter.
0: DC/DC2 is disabled.
1: DC/DC2 is enabled.

REGISTER STAT1
A signal/alert is currently active.

	7	6	5	4	3	2	1	0
	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
	r	r	r	r	r	r	r	r
	0	0	0	0	0	0	0	0

Bit 7: Reserved, do not use.
Bit 6, TW: Thermal warning of the chip.
0: Alert is not active.
1: Alert is active.
Bit 5, LEDTSD: LED Thermal shutdown. Is active if the voltage on the TLED pin is above TLEDTSDTH + TLED_TSDTH_HYST threshold. Becomes false if the TLED voltage drops below TLEDTSDTH − TLED_TSDTH_HYST.
0: Alert is not active.
1: Alert is active.
Bit 4, LEDTW: LED Thermal warning. Is active if the voltage on the TLED pin is above TLEDTWTH + TLED_TWTH_HYST threshold. Becomes false if the TLED voltage drops below TLEDWTH − TLED_TWTH_HYST.
0: Alert is not active.
1: Alert is active.
Bit 3, LEDOV: LED Overvoltage. Is active if the voltage on the VLED pin is above VLEDOVTH + VLED_OVTH_HYST threshold. Becomes false if the VLED voltage drops below VLEDOVTH − VLED_OVTH_HYST.
0: Alert is not active.
1: Alert is active.
Bit 2, LEDUV: LED Undervoltage. Is active if the voltage on the VLED pin is below VLEDUVTH − VLED_UVTH_HYST threshold. Becomes false if the VLED voltage is above VLEDUVTH + VLED_UVTH_HYST.
0: Alert is not active.
1: Alert is active.
Bit 1, VDD2OC: VDD2 Overcurrent. Is active if the IDD2 current is above VDD2OCTH + VDD2_OCTH_HYST threshold. Becomes false if the VDD2OCTH current is below VDD2_OCTH_UVTH + VDD2_OCTH_HYST.
0: Alert is not active.
1: Alert is active.
Bit 0, VDD1OC: VDD1 Overcurrent. Is active if the IDD1 current is above a fixed limit.
0: Alert is not active.
1: Alert is active.

REGISTER STAT2

A signal/alert is currently active.

	7	6	5	4	3	2	1	0
	Rsv.					LEDOC	LEDNOK	VDD2NOK
	r					r	r	r
	0					0	0	0

Bits 3–7: Reserved, do not use.

Bit 2, LEDOC: LED Overcurrent. Is active if this condition is true: ILED x Rsns > 0.382.
In reality, when this limit is crossed, a comparator will react in a matter of nanoseconds and turn off the LED driver.
The LED current will drop immediately and the LEDOC bit in this register will be cleared before the MCU can read it and the LEDOC bit in the STATP register will be set indicating a LED overcurrent event occured.
0: Alert is not active.
1: Alert is active.

Bit 1, LEDNOK: LED desaturation error. Is active if a severe error occured in one of the switching transistors of the LED driver.
In reality, when this limit is crossed, a comparator will react in a matter of nanoseconds and turn off the LED driver.
The LED current will drop immediately and the LEDNOK bit in this register will be cleared before the MCU can read it and the LEDNOK bit in the STATP register will be set indicating there is a severe issue with the transistors.
This error indicates something is wrong with the hardware of the LED driver.
0: Alert is not active.
1: Alert is active.

Bit 0, VDD2NOK: VDD2 desaturation error. True if a severe error occured in of the switching transistors of the DC/DC2 converter.
In reality, when this limit is crossed, a comparator will react in a matter of nanoseconds and turn off the DC/DC1.
The VDD2 current will drop immediately and the VDD2NOK bit in this register will be cleared before the MCU can read it and the VDD2NOK bit in the STATP register will be set indicating there is a severe issue with the transistors.
This error indicates something is wrong with the hardware of the VDD2 DC/DC1.
0: Alert is not active.
1: Alert is active.

REGISTER STATP1

A signal has become active since the last read to this register.

	7	6	5	4	3	2	1	0
	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
	r	r	r	r	r	r	r	r
	0	0	0	0	0	0	0	0

Bit 7: Reserved, do not use.

Bit 6, TW: Thermal warning of the chip.
0: Alert is not active.
1: Alert is active.

Bit 5, LEDTSD: LED Thermal shutdown. True as long as the voltage on the TLED pin is above TLEDTSDTH + TLED_TSDTH_HYST threshold. Becomes false if the TLED voltage drops below TLEDTSDTH − TLED_TSDTH_HYST.
0: Alert is not active.
1: Alert is active.

Bit 4, LEDTW: LED Thermal warning. True as long as the voltage on the TLED pin is above TLEDTWTH + TLED_TWTH_HYST threshold. Becomes false if the TLED voltage drops below TLEDWTH − TLED_TWTH_HYST.
0: Alert is not active.
1: Alert is active.

Bit 3, LEDOV: LED Overvoltage. True as long as the voltage on the VLED pin is above VLEDOVTH + VLED_OVTH_HYST threshold. Becomes false if the VLED voltage drops below VLEDOVTH − VLED_OVTH_HYST.
0: Alert is not active.
1: Alert is active.

Bit 2, LEDUV: LED Undervoltage. True as long as the voltage on the VLED pin is below VLEDUVTH − VLED_UVTH_HYST threshold. Becomes false if the VLED voltage is above VLEDUVTH + VLED_UVTH_HYST.
0: Alert is not active.
1: Alert is active.

Bit 1, VDD2OC: VDD2 Overcurrent. True as long as the IDD2 current is above VDD2OCTH + VDD2_OCTH_HYST threshold. Becomes false if the VDD2OCTH current is below VDD2_OCTH_UVTH + VDD2_OCTH_HYST.
0: Alert is not active.
1: Alert is active.

Bit 0, VDD1OC: VDD1 Overcurrent. True as long as the IDD1 current is above a fixed limit of ....
0: Alert is not active.
1: Alert is active.

REGISTER STATP2

A signal has become active since the last read to this register.

	7	6	5	4	3	2	1	0
	Rsv.					LEDOC	LEDNOK	VDD2NOK
	r					r	r	r
	0					0	0	0

Bits 3–7: Reserved, do not use.

Bit 2, LEDOC: LED Overcurrent. True as long as this condition is true: ILED x Rsns > 0.382.
In reality, when this limit is crossed, a comparator will react in a matter of nanoseconds and turn off the LED driver.
The LED current will drop immediately and the LEDOC bit in this register will be cleared before the MCU can read it and the LEDOC bit in the STATP register will be set indicating a LED overcurrent event occured.
0: Alert is not active.
1: Alert is active.

Bit 1, LEDNOK: LED desaturation error. True if a severe error occured in of the switching transistors of the LED driver.
In reality, when this limit is crossed, a comparator will react in a matter of nanoseconds and turn off the LED driver.
The LED current will drop immediately and the LEDNOK bit in this register will be cleared before the MCU can read it and the LEDNOK bit in the STATP register will be set indicating there is a severe issue with the transistors.
This error indicates something is wrong with the hardware of the LED driver.
0: Alert is not active.
1: Alert is active.

Bit 0, VDD2NOK: VDD2 desaturation error. True if a severe error occured in of the switching transistors of the DC/DC2 converter.
In reality, when this limit is crossed, a comparator will react in a matter of nanoseconds and turn off the DC/DC1.
The VDD2 current will drop immediately and the VDD2NOK bit in this register will be cleared before the MCU can read it and the VDD2NOK bit in the STATP register will be set indicating there is a severe issue with the transistors.
This error indicates something is wrong with the hardware of the VDD2 DC/DC1.
0: Alert is not active.
1: Alert is active.

REGISTER STATN1

A signal has become inactive since the last read to this register.

	7	6	5	4	3	2	1	0
	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
	r	r	r	r	r	r	r	r
	0	0	0	0	0	0	0	0

This register has the same structure as STATP1; refer there for more information.

REGISTER STATN2

A signal has become inactive since the last read to this register.

	7	6	5	4	3	2	1	0
	Rsv.					LEDOC	LEDNOK	VDD2NOK
	r					r	r	r
	0					0	0	0

This register has the same structure as STATP2; refer there for more information.

REGISTER INTP1

Interrupt enable register for STATP1. Defines which alert signals, if they become active, result in an interrupt condition on the INTB line.

	7	6	5	4	3	2	1	0
	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
	0	0	0	0	0	0	0	0

Bit 7: Reserved, do not use.
Bit 6, TW: Thermal warning.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 5, LEDTSD: LED Thermal shutdown.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 4, LEDTW: LED Thermal warning.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 3, LEDOV: LED Overvoltage.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 2, LEDUV: LED Undervoltage.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 1, VDD2OC: VDD2 Overcurrent.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 0, VDD1OC: VDD1 Overcurrent.
0: Interrupt disabled/masked.
1: Interrupt enabled.

REGISTER INTP2

Interrupt mask register for STATP2. Defines which alert signals, if they become active, result in an interrupt condition on the INTB line.

	7	6	5	4	3	2	1	0
	Rsv.					LEDOC	LEDNOK	VDD2NOK
	r					r/w	r/w	r/w
	0					0	0	0

Bits 3–7: Reserved, do not use.
Bit 2, LEDOC: LED Overcurrent.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 1, LEDNOK: LED desaturation error.
0: Interrupt disabled/masked.
1: Interrupt enabled.
Bit 0, VDD2NOK: VDD2 desaturation error.
0: Interrupt disabled/masked.
1: Interrupt enabled.

REGISTER INTN1

Interrupt enable register for STATN1. Defines which alert signals, if they become active, result in an interrupt condition on the INTB line.

	7	6	5	4	3	2	1	0
	Rsv.	TW	LEDTSD	LEDTW	LEDOV	LEDUV	VDD2OC	VDD1OC
	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
	0	0	0	0	0	0	0	0

This register has the same structure as INTP1; refer there for more information.

REGISTER INITN2

Interrupt mask register for STATN2. Defines which alert signals, if they become active, result in an interrupt condition on the INTB line.

	7	6	5	4	3	2	1	0
	Rsv.					LEDOC	LEDNOK	VDD2NOK
	r					r/w	r/w	r/w
	0					0	0	0

This register has the same structure as INTP2; refer there for more information.

REGISTER VBB

VBB−GND voltage measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

Bits 6–15, ADCv: ADC value.
Bits 0–5: Reserved, do not use.

REGISTER IBB

IBB current measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

Bits 6–15, ADCv: ADC value.
Bits 0–5: Reserved, do not use.

REGISTER VDD1

VDD1 voltage measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

This register has the same structure as IBB; refer there for more information.

REGISTER IDD1
IDD1 current measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

This register has the same structure as IBB; refer there for more information.

REGISTER VDD2
VDD2 voltage measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

This register has the same structure as IBB; refer there for more information.

REGISTER IDD2
IDD2 current measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

This register has the same structure as IBB; refer there for more information.

REGISTER VLED
VLED current measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

This register has the same structure as IBB; refer there for more information.

REGISTER ILED
ILED current measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

This register has the same structure as IBB; refer there for more information.

REGISTER TLED
TLED voltage measurement.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCv										Rsv.					
r										r					
0										0					

This register has the same structure as IBB; refer there for more information.

REGISTER VDD10CTH
VDD1 overcurrent threshold register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
val										Rsv.					
r/w										r					
$3FF_H$										$3F_H$					

Bits 6–15, val: value.
1023: The detection is disabled.
Bits 0–5: Reserved, do not use.

REGISTER VDD2OCTH
VDD2 overcurrent threshold register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
val										Rsv.					
r/w										r					
$3FF_H$										$3F_H$					

This register has the same structure as VDD1OCTH; refer there for more information.

REGISTER TLEDTWTH
TLED thermal warning threshold register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
val										Rsv.					
r/w										r					
$3FF_H$										$3F_H$					

This register has the same structure as VDD1OCTH; refer there for more information.

REGISTER TLEDTSDTH
TLED thermal shutdown threshold register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
val										Rsv.					
r/w										r					
$3FF_H$										$3F_H$					

This register has the same structure as VDD1OCTH; refer there for more information.

REGISTER VLEDOVTH
VLED overvoltage threshold register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
val										Rsv.					
r/w										r					
$3FF_H$										$3F_H$					

This register has the same structure as VDD1OCTH; refer there for more information.

REGISTER VLEDUVTH
VLED undervoltage threshold register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
val										Rsv.					
r/w										r					
$3FF_H$										$3F_H$					

This register has the same structure as VDD1OCTH; refer there for more information.

REGISTER VDD1OCTH_HYS
Overcurrent threshold hysteresis register.

	7	6	5	4	3	2	1	0
	Rsv.	val						
	r	r/w						
	0	$0A_H$						

Bit 7: Reserved, do not use.
Bits 0–6, val: value.

REGISTER VDD2OCTH_HYS
Overcurrent threshold hysteresis register.

	7	6	5	4	3	2	1	0
	Rsv.	val						
	r	r/w						
	0	$0A_H$						

Bit 7: Reserved, do not use.
Bits 0–6, val: value.

REGISTER TLEDTWTH_HYS
LED thermal warning threshold hysteresis register.

	7	6	5	4	3	2	1	0
	Rsv.	val						
	r	r/w						
	0	$0A_H$						

This register has the same structure as VDD2OCTH_HYS; refer there for more information.

REGISTER TLEDTSDTH_HYS
TLED thermal shutdown threshold hysteresis register.

	7	6	5	4	3	2	1	0
	Rsv.	val						
	r	r/w						
	0	$0A_H$						

This register has the same structure as VDD2OCTH_HYS; refer there for more information.

REGISTER VLEDOVTH_HYS
VLED overvoltage threshold hysteresis register.

	7	6	5	4	3	2	1	0
	Rsv.	val						
	r	r/w						
	0	$0A_H$						

This register has the same structure as VDD2OCTH_HYS; refer there for more information.

REGISTER VLEDUVTH_HYS
VLED undervoltage threshold hysteresis register.

	7	6	5	4	3	2	1	0
	Rsv.	val						
	r	r/w						
	0	$0A_H$						

This register has the same structure as VDD2OCTH_HYS; refer there for more information.

REGISTER INTDIM
Internal DIM register.

	7	6	5	4	3	2	1	0
	EN	DACv						
	r/w	r/w						
	0	0						

Bit 7, EN: Internal DIM enable.
0: The internal DIM is disabled.
1: The internal DIM is enabled.

Bits 0–6, DACv: Internal DAC value.

REGISTER LEDFC

LED driver switching frequency register.

	7	6	5	4	3	2	1	0
	JIT_EN	FREQ						
	r/w	r/w						
	0	4						

Bit 7, JIT_EN: Spread spectrum enable.
- 0: Spread spectrum disabled.
- 1: Spread spectrum enabled.

Bits 0–6, FREQ: Switching frequency value.
- 0: 1 MHz switching frequency.
- 1: 800 kHz switching frequency.
- 2: 666 kHz switching frequency.
- 3: 571 kHz switching frequency.
- 4: 500 kHz switching frequency.
- 5: 444 kHz switching frequency.
- 6: 400 kHz switching frequency.
- 7: 363 kHz switching frequency.
- 8: 333 kHz switching frequency.
- 9: 307 kHz switching frequency.
- 10: 285 kHz switching frequency.
- 11: 250 kHz switching frequency.
- 12: 235 kHz switching frequency.
- 13: 210 kHz switching frequency.
- 14: 190 kHz switching frequency.
- 15: 173 kHz switching frequency.

REGISTER SLCMP

LED driver slope compensation register.

	7	6	5	4	3	2	1	0
	Rsv.				SLP2		SLP1	
	r				r/w		r/w	
	0				2		2	

Bits 4–7: Reserved, do not use.

Bits 2–3, SLP2: Slope compensation applicable when LED driver is operating in 50% to 100% duty−cycle range.
- 0: 0.3 V/μs
- 1: 0.4 V/μs
- 2: 0.6 V/μs
- 3: 0.9 V/μs

Bits 0–1, SLP1: Slope compensation applicable when LED driver is operating in 0 to 50% duty−cycle range.
- 0: 0.1 V/μs
- 1: 0.2 V/μs
- 2: 0.3 V/μs
- 3: 0.4 V/μs

REGISTER MPS

Maintain Power Signature register.

	7	6	5	4	3	2	1	0
	EN	DELTA						
	r/w	r/w						
	1	4						

Bit 7, EN: MPS enable.
0: MPS disabled.
1: MPS enabled.

Bits 0–6, DELTA: Define how long the MPS pulse lasts. The minimum MPS pulse is about 7 ms if LCF bit is active and 75 ms if the LCF bit is disabled.
The DELTA value defines how many ms are added to the minimum MPS time.
0: Add 0 ms to the minimum MPS pulse.
63: Add 63 ms to the minimum MPS pulse.
127: Add 127 ms to the minimum MPS pulse.

REGISTER FDEV

Frequency Deviation register.

	7	6	5	4	3	2	1	0
	Rsv.	SSLUT_DIS		Rsv.		FDEV		
	r	r/w		r		r/w		
	0	0		0		6		

Bit 7: Reserved, do not use.

Bits 5–6, SSLUT_DIS: Spread Spectrum Look−up Table Disable.
0: The FDEV and FMOD field values are directly used for the spread spectrum block (expert mode). The user is responsible for calculating the amount of spread.
1: The spread spectrum block calculates the needed deviation and modulation values to achieve a certain amount of spread (%) based on the FDEV and FMOD field values. The relation between FMOD/FDEV and the amount of spread (%) is given in a lookup table.

Bits 3–4: Reserved, do not use.

Bits 0–2, FDEV: Frequency Deviation value.
0: 1.8 MHz deviation.
1: 914 kHz deviation.
2: 479 kHz deviation.
3: 322 kHz deviation.
4: 246 kHz deviation.
5: 165 kHz deviation.
6: 100 kHz deviation.
7: 56 kHz deviation.

REGISTER FMOD

Frequency Modulation register.

	7	6	5	4	3	2	1	0
	Rsv.						val	
	r						r/w	
	0						1	

Bits 2–7: Reserved, do not use.

Bits 0–1, val: Frequency Modulation value.

0: 200 Hz modulation.

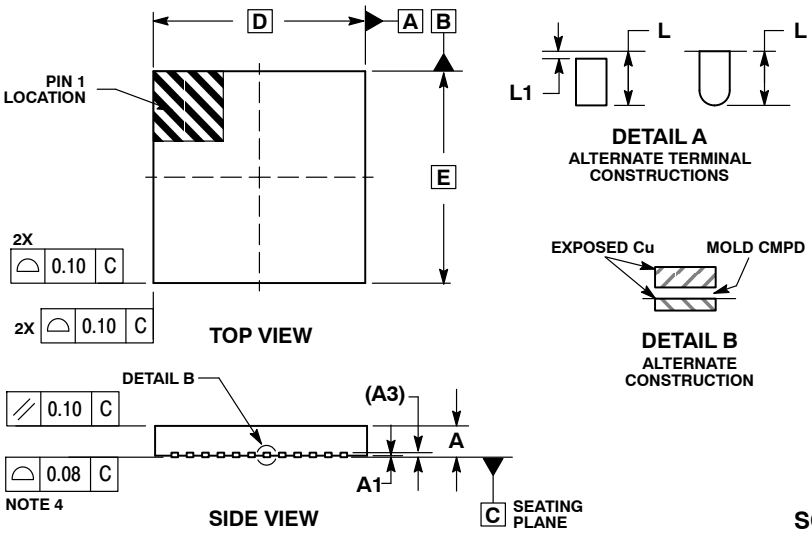
1: 400 Hz modulation.

2: 800 Hz modulation.

3: 1600 Hz modulation.

PACKAGE DIMENSIONS

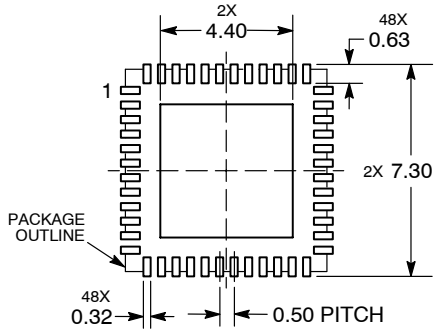
QFN48 7x7, 0.5P
CASE 485EP
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	7.00 BSC	
D2	4.00	4.20
E	7.00 BSC	
E2	4.00	4.20
e	0.50 BSC	
L	0.30	0.50
L1	0.00	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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