110 V 2.5 A Single Channel Floating Gate Drivers with Desaturation Protection and Charge Pump

FAD3151MXA, FAD3171MXA

The FAD3151MXA and FAD3171MXA are single channel floating automotive gate drivers suitable for driving high−speed power MOSFETs up to 110 V. Designed in a SOI technology, the drivers are ideal for applications that require noise immunity against severe negative transients and ground offset up to −80 V.

The FAD3151MXA/71 drivers have an integrated desaturation detection to protect the power switches during short−circuit and over−current conditions. The drivers are also equipped with a soft shutdown feature, which initiates a soft shutdown of driver outputs upon desat detection, thus preventing possible overvoltage across power MOSFETs during a heavy−load condition.

The FAD3151MXA/71 drivers are equipped with bidirectional fault reporting pin that can generate a fault output during desat and under−voltage lockout (UVLO) condition. The bidirectional nature of the fault−reporting pin allows the driver to respond to external fault commands, thereby facilitating fault communication across the system. In addition, the FAD3171MXA has an integrated charge pump to support 100% duty cycle operation of high side MOSFETs.

In summary, the FAD3151MXA/71 are versatile drivers with features like desat detection, soft shutdown, fault reporting capability, UVLO protection, and charge pump.

Features

- Single Channel Gate Driver with 110 V floating Vs capability
- Negative Transient Capability up to −80 V
- 2.5 A Output Source and Sink Current
- MOSFET Drain−Source Desaturation Detection with Soft Shutdown
- Integrated Charge Pump to support 100% Duty Cycle Operation (FAD3171MXA only)
- Under−voltage Lock Out for both Input Logic and Output Stage
- Bi−directional Fault Reporting Pin
- High Speed Driver with Short Propagation Delay
- dV_s/dt Immune to min ±50 V/ns
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{DD} Swing on Input Pins
- SOIC−8 package
- Automotive Qualified to AEC Q100
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Gate Driver for 80V and 100V MOSFETs
- 48 V Belt Starter Generator
- 48 V Auxiliary Motor Control (A/C compressor, e−turbo, …)
- 48 V Battery Switches
- 48 V DC−DC converter
- PTC Heater, Active Discharge Circuit etc.

SOIC−8
CASE 751EB

ORDERING INFORMATION

Device	Package	Shipping†
FAD3151MXA	SOIC−8 (Pb−Free)	Tape & Reel
FAD3171MXA	SOIC−8 (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SAFETY SUPPORT

Support integration into customer's safety application with a set of safety documents including FMEDA and a hardware−software interface document.

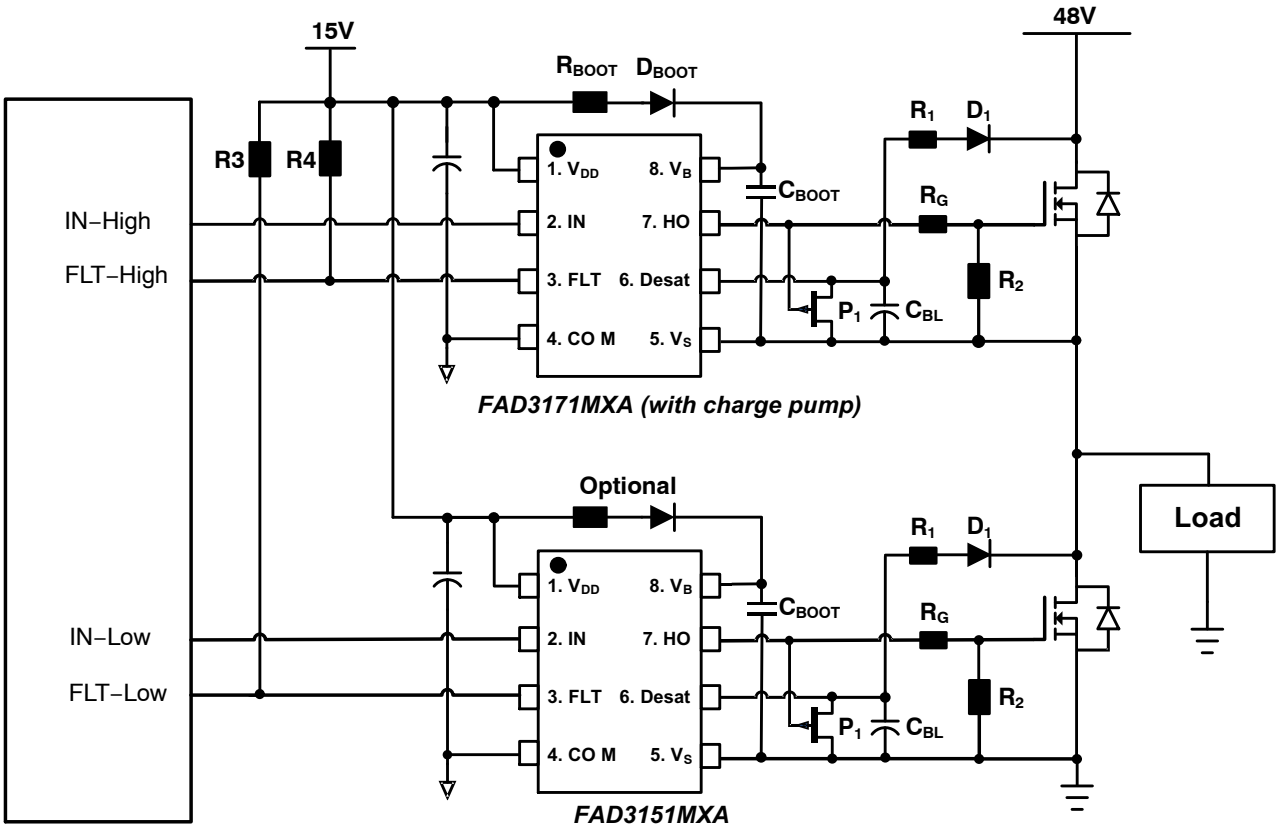


Figure 1. Application Schematic with FAD3171MXA as High Side and FAD3151MXA as Low Side drivers

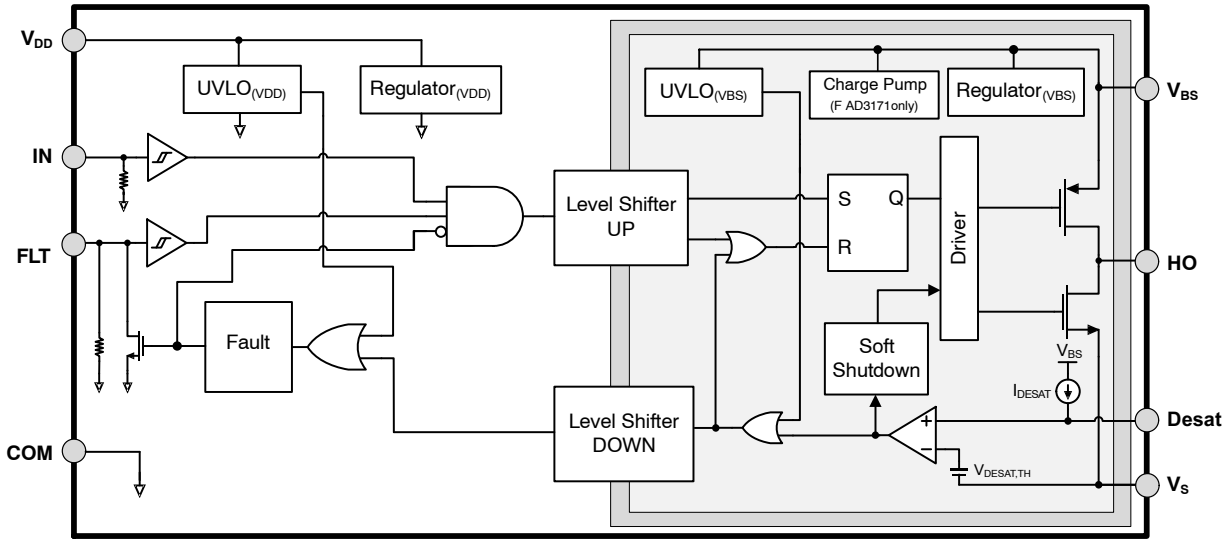


Figure 2. FAD3151MXA and FAD3171MXA (with charge pump) Block Diagram

PIN FUNCTION DESCRIPTION

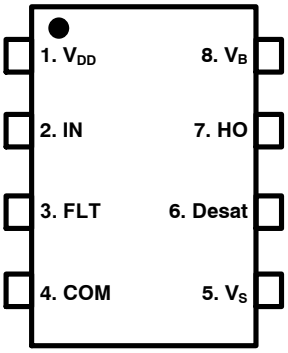


Figure 3. Pin Connection
(Top View)

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Description
1	V_{DD}	Power supply for logic stage
2	IN	Input command
3	FLT	Bi−directional fault pin
4	COM	Ground for logic stage
5	V_S	Floating source connection
6	Desat	Drain to source desaturation detection pin
7	HO	Output
8	V_B	Floating power supply for power stage

MAXIMUM RATINGS

T_A = −40°C ~ 125°C unless otherwise noted. Voltage potentials are referenced to COM unless otherwise noted.

Rating	Symbol	Value	Unit
Logic Power Supply	V_{DD}	−0.3 to 20	V
Logic Input Voltage (IN, FLT)	V_{IN}	−0.3 to (V_{DD} + 0.3)	V
Floating Source Voltage	V_S	−115 to 115	V
Floating Bootstrap Supply Voltage	V_B	(V_S − 0.3) to (V_S + 20)	V
Output Voltage	V_{HO}	(Vs − 0.3) to (V_B + 0.3)	V
Desaturation Voltage	V_{DESAT}	(Vs − 0.3) to (V_B + 0.3)	V
Allowable Offset Voltage Slew Rate	dVs/dt	+/−50	V/ns
Maximum Junction Temperature	T_J	150	°C
Thermal Resistance, Junction−to−Ambient (Note 1)	Rth_{JA}	200	°C/W
Power Dissipation at T_A= 25°C	P_D	0.625	W
Storage Temperature Range	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	500 for all pins	V
		750 for corner pins	
Moisture Sensitivity Level	MSL	3	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to the following standards:
   JESD51−2: Integral circuits thermal test method environmental conditions − natural convection
   JESD51−3: Low effective thermal conductivity test board for leaded surface mount packages
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001−2012
   ESD Charged Device Model tested per JESD22−C101
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

RECOMMENDED OPERATING RANGES

T_A = −40°C ~ 125°C unless otherwise noted. Voltage potentials are referenced to COM unless otherwise noted.

Rating	Symbol	Min	Max	Unit
Power Supply	V_{DD}	V_{DDUV+}	18	V
Logic Input Voltage (IN, FLT)	V_{IN}	0	18	V
High−Side Vs Floating Supply Offset Voltage	V_S	−80	110	V
High−side V_{BS} Bootstrap Voltage	V_{BS}	V_{BSUV+}	18	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_S = 0 V unless otherwise noted, T_A = −40°C to 125°C. Voltage potentials are referenced to COM unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POWER SUPPLY SECTION						
V_{BS} Under−Voltage Positive−going Threshold		V_{BSUV+}	6	8	10.5	V
V_{BS} Under−Voltage Negative−going Threshold		V_{BSUV-}	5.5	7.5	9.7	
V_{BS} Slew Rate During Startup (Note 4)		$V_{BS(SR)}$	2.5			V/ms
V_{DD} Under−Voltage Positive−going Threshold		V_{DDUV+}			6	V
V_{DD} Under−Voltage Negative−going Threshold		V_{DDUV-}	2.2	3.9		
Offset Supply Leakage Current	V_B = V_S = 80 V	I_{LK1}			5	μA
Quiescent V_{DD} Supply Current	V_{IN} = 0 V or 5 V	I_{QDD}		270	500	μA
Quiescent V_{BS} Supply Current	V_{IN} = 0 V or 5 V	I_{QBS}		525	1000	
Operating V_{DD} Supply Current	V_{IN} = 0 V or 5 V; f_{SW} = 20 kHz; C_L = 1 nF	I_{PDD}		250	600	
Operating V_{BS} Supply Current	V_{IN} = 0 V or 5 V; f_{SW} = 20 kHz; C_L = 1 nF	I_{PBS}		1000	2000	

4. This limitation applies only to temperatures exceeding 105°C.

LOGIC INPUT SECTION						
Logic “1” Input threshold for IN, FLT		V_{IH}		2.1	2.5	V
Logic “0” Input threshold for IN, FLT		V_{IL}	1.3	1.7		
Logic Input High Bias Current	V_{IN} = 5 V	I_{IN+}		48	70	μA
Logic Input Low Bias Current	V_{IN} = 0 V	I_{IN-}			2	μA
Input Pull−down Resistance		R_{IN}		80		kΩ
FAULT SECTION						
Fault Output Internally pulled down voltage level	10 kΩ pull up resistor to V_{DD}, V_{DESAT} > V_{DESAT+}	V_{FLT+}			200	mV
Fault Output Not Internally pulled down voltage level	10 kΩ pull up resistor to V_{DD}, V_{DESAT} < V_{DESAT+}	V_{FLT-}		13.8		V
Fault Pin Pull−down Resistance		R_{FLT}		110		kΩ
Desaturation High detection threshold (Note 5)		$V_{DESAT,TH}$	2.3	3.0	4	V
Desaturation Bias Current		I_{DESAT}	180	320	430	μA

5. The actual desaturation threshold at the Power MOSFET can be adjusted to a value lower than $V_{DESAT,TH}$ with an external resistor (see Application Note)

GATE DRIVER OUTPUT SECTION						
High−Level Output Voltage (V_B − V_{HO})	V_{IN} = 5 V, No Load	V_{HOH}			50	mV
Low−Level Output Voltage (V_{HO}−V_S)	V_{IN} = 0 V, No Load	V_{HOL}			50	mV
Source Peak Pulsed Current (Note 6)	V_{IN} = 5 V, V_{HO} = 0 V, Pulse Width ≤10 μs	I_{O+}		2.5		A
Sink Peak Pulsed Current (Note 6)	V_{HO} = V_{BS}= 15 V, Pulse Width ≤10 μs	I_{O-}		2.5		
Allowable Negative V_S pin voltage, with signal Propagation Capability from IN to HO		V_S	−80			V
Driver Output Pull−up Resistance	I_{OUT} = 90 mA (DC)	R_{OH}		3		Ω
Driver Output Pull−down Resistance	I_{OUT} = 90 mA (DC)	R_{OL}		1.2		Ω

6. Guaranteed by design

ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_S = 0 V unless otherwise noted, T_A = −40°C to 125°C. Voltage potentials are referenced to COM unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CHARGE PUMP SECTION [FAD3171MXA only]						
Turn on threshold level, referenced to V_{BS}	V_{DD} > V_{DDUV+}, R_L = 100 kΩ, V_S = 48 V	CP_{ON}	7.9	10.8	15.2	V
Turn off threshold level, referenced to V_{BS}		CP_{OFF}	8.3	11.2	15	V
Charge Pump V_{BS} hysteresis		CP_{HYS}		0.4		V
Delta (CP_{ON} − V_{BSUV-}) (Note 7)	V_{DD} > V_{DDUV+}, R_L=100 kΩ, V_S = 48 V	$\Delta_{CP,VBSUV-}$	1			V
Charge Pump Supply Voltage		$V_{S,CP}$	24			V
Charge Pump Output Current capability (Note 8)	V_{BS} = CP_{ON}, V_S > $V_{S,CP}$	$I_{CP,OUT}$			150	μA
Charge Pump Oscillation Frequency (Note 6)		CP_{fs}			5.5	MHz

7. Difference between the charge−pump turn on threshold and V_{BS} under−voltage negative−going threshold.
8. Net output current, excluding the internal current consumption of the gate driver in steady state.

DYNAMIC SECTION

Input pulse filtering time (Note 9)		T_{IN_FILT}		40		ns
Turn−On Propagation Delay	V_S = 0 V, C_L = 1000 pF	t_{ON}		50	100	ns
Turn−Off Propagation Delay	V_S = 0 V, C_L = 1000 pF	t_{OFF}		50	100	ns
Turn−On Rise Time	Vs = 0 V, C_L = 1000 pF	t_R		15	25	ns
Turn−Off Fall Time		t_F		10	20	ns
V_{DD} and V_{BS} Under−Voltage filtering time (Note 6)	V_{DD} < V_{DDUV-} or V_{BS}< V_{BSUV-} to V_{HO} falls by 10%	t_{VDDUV} t_{VBSUV}		10		μs
External FLT Pulse Width (Note 10)	V_{FLT} < V_{IL} to V_{HO} falls by 10%	t_{FLT_Pulse}	3			μs
Desat detection to HO propagation delay	V_{DESAT} > V_{DESAT+} to V_{HO} falls by 10% with R_L= 0 Ω and C_L = 1 nF	T_{DESAT_HO}		75	110	ns
Desat detection to FLT propagation delay	V_{DESAT} > $V_{DESAT,TH}$ to V_{FLT} < V_{FLT-}	T_{DESAT_FLT}		80	110	ns
FLT Locking Duration	Desaturation or UVLO detected	t_{FLT_LO}	150	550		μs
Soft shutdown resistance		R_{SOFT}		170		Ω

9. Shorter input pulses are filtered out and do not cause the output to change state.
10. The pulse width of the external fault signal at which the driver output turns off.

TYPICAL CHARACTERISTICS

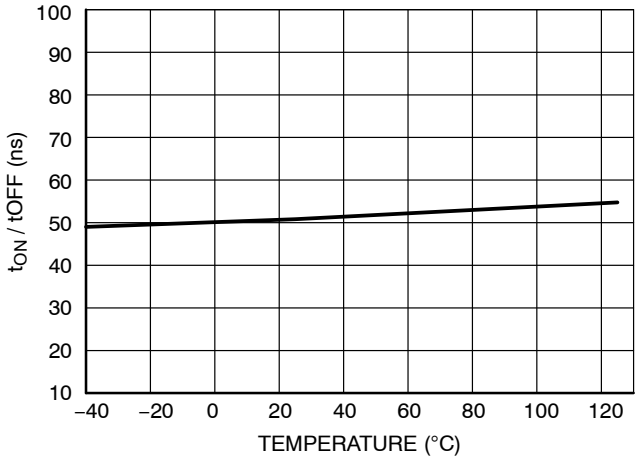


Figure 4. Propagation Delay vs. Temperature

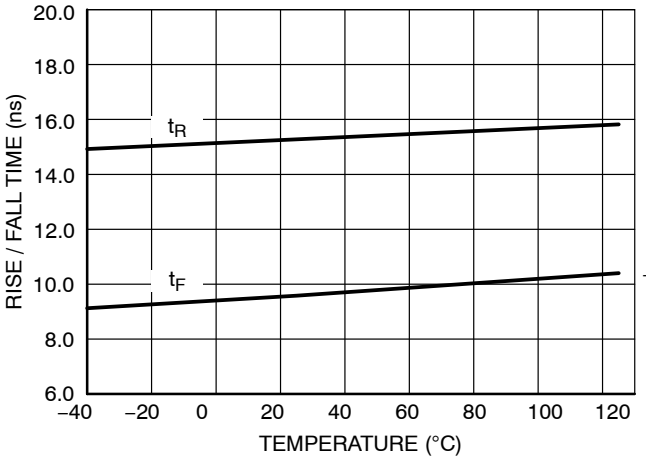


Figure 5. Rise Time vs. Temperature

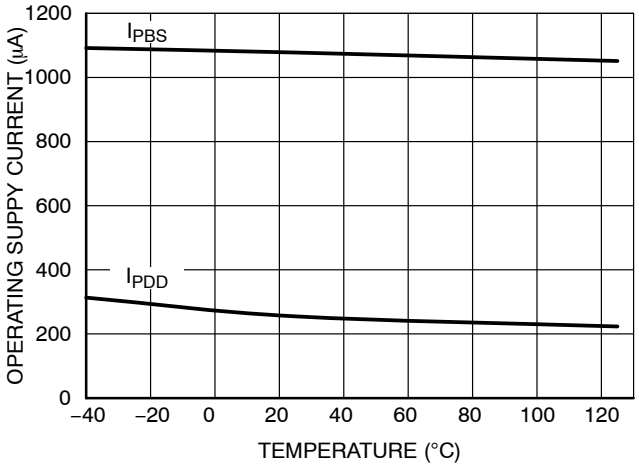


Figure 6. Operating Supply Current vs. Temperature

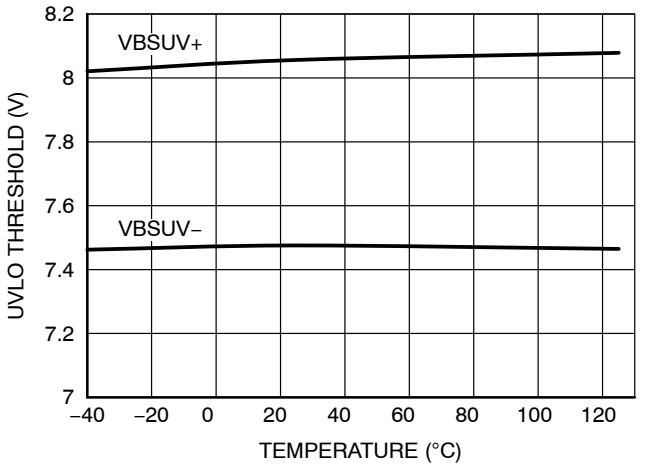


Figure 7. VBS UVLO vs. Temperature

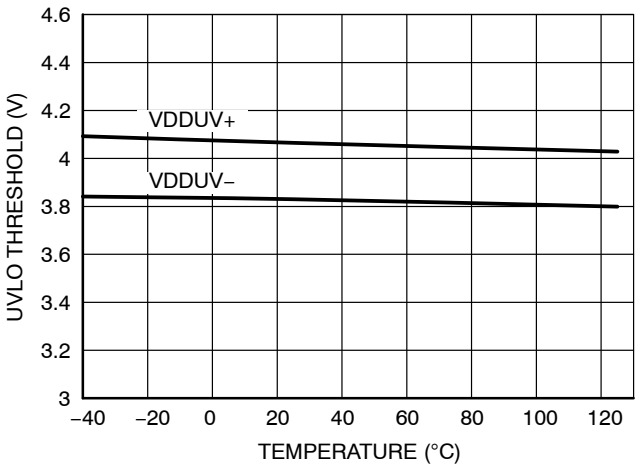


Figure 8. VDD UVLO vs. Temperature

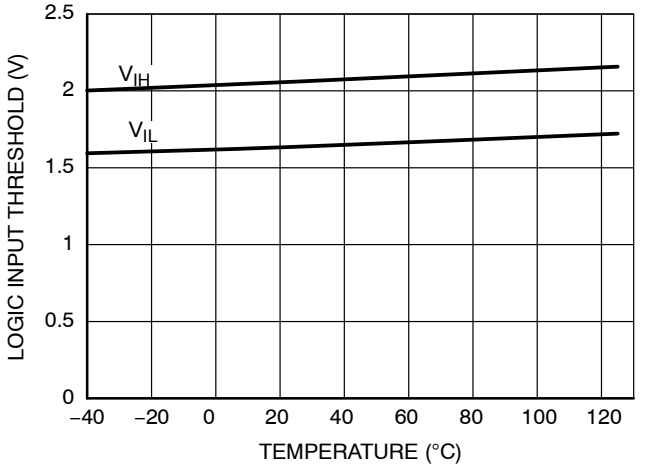


Figure 9. Logic Input Voltage vs. Temperature

TYPICAL CHARACTERISTICS

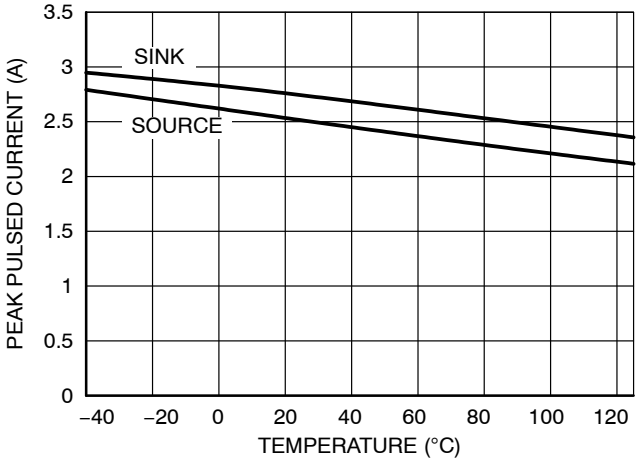


Figure 10. Peak Pulsed Current vs. Temperature

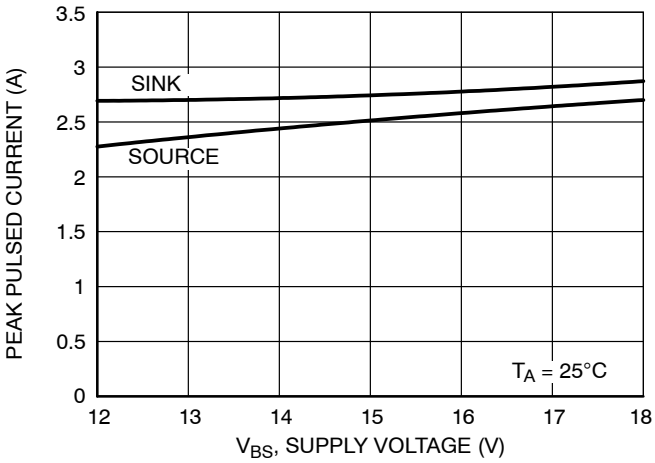


Figure 11. Peak Pulsed Current vs. VBS Voltage

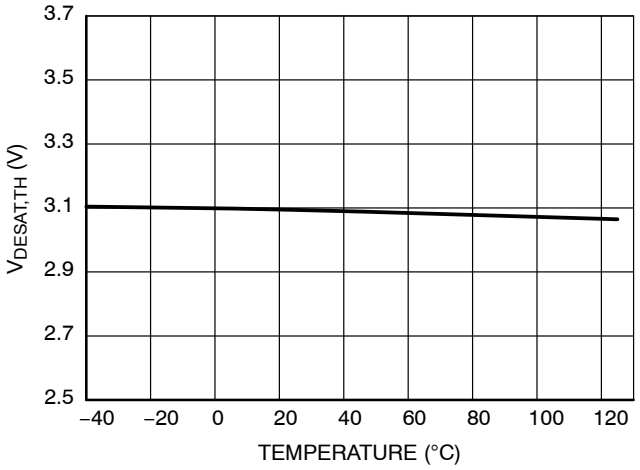


Figure 12. Desat Threshold vs. Temperature

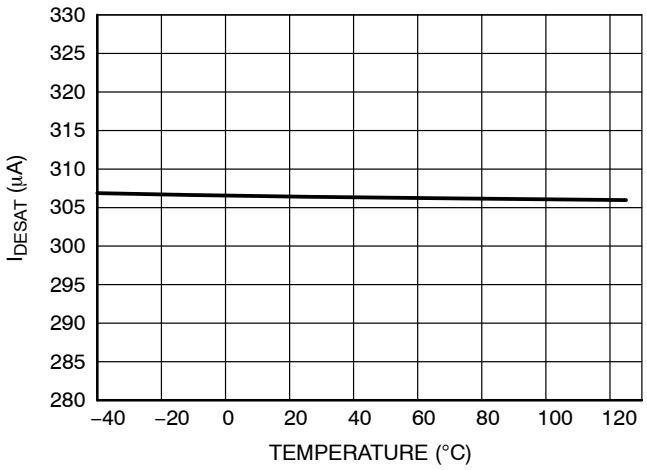


Figure 13. Desat Current vs. Temperature

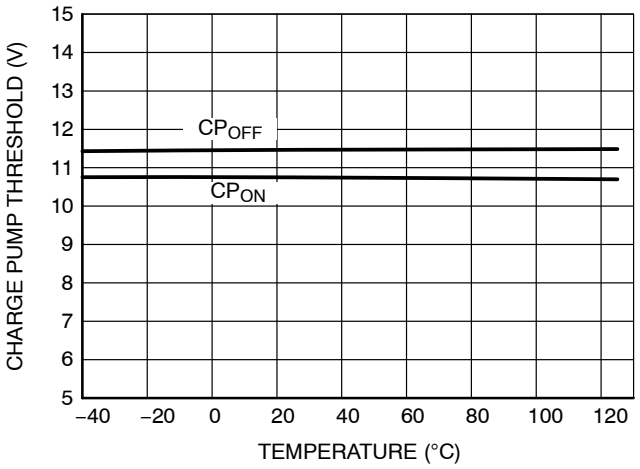


Figure 14. Charge Pump Turn On/Turn Off Threshold vs. Temperature

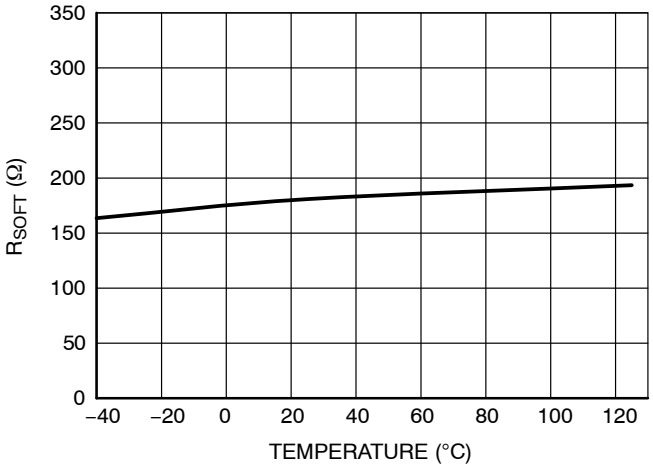


Figure 15. Soft Shutdown Resistance vs. Temperature

GATE DRIVER DESCRIPTION

Figure 2 shows the block diagram of the FAD3151MXA and FAD3171MXA (with charge pump). The section below describes the functional characteristics of 3151/71 gate drivers.

Input and Fault Signal Buffer

The driver includes input and fault signal buffers to avoid parasitic triggering due to noises at input and fault pins. The input pin has a 40 ns filter, which means the driver output will not change its state for an input pulse shorter than 40 ns. Similarly, the fault pin has a 3 μs filter, which means the driver output will not change its state for an external fault pulse shorter than 3 μs.

VDD and VBS Under Voltage Lock Out

The gate driver has UVLO monitoring circuits with a 10 μs filter for both V_{DD} and V_{BS} power supplies. If the V_{DD} or V_{BS} voltages were to drop below their respective UVLO threshold:

- Within the first 10 μs of an under−voltage condition (see Figure 16):
  - The gate driver does not take any action and the output follows the input as expected.
- After 10 μs of under−voltage condition, the UVLO circuit triggers a fault for a period equal to FLT locking duration:
  - If the under−voltage condition lasts for a duration shorter than the FLT locking duration, the fault pin is released after the FLT locking duration is over, upon which the driver output will begin to follow the input logic as expected (see Figure 17).
  - If the under−voltage condition lasts for a duration longer than the FLT locking duration, the fault pin is released only after the under−voltage condition has disappeared. The driver output will begin to follow the input logic once the fault pin is released (see Figure 18).

The figures below show examples of driver functionality during various under−voltage conditions of the V_{BS} supply; note that the same description applies for an under−voltage condition of the V_{DD} supply.

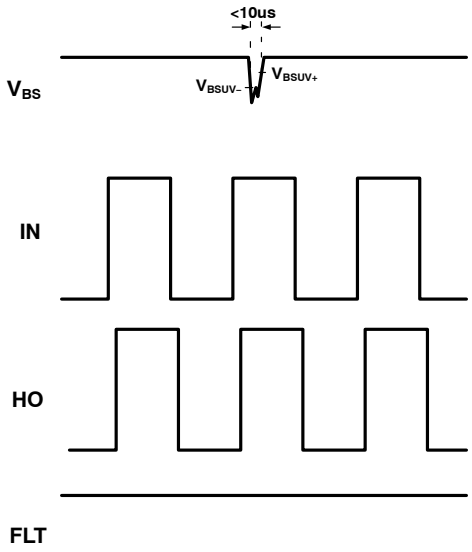


Figure 16. Under−Voltage Condition Shorter than 10 μs

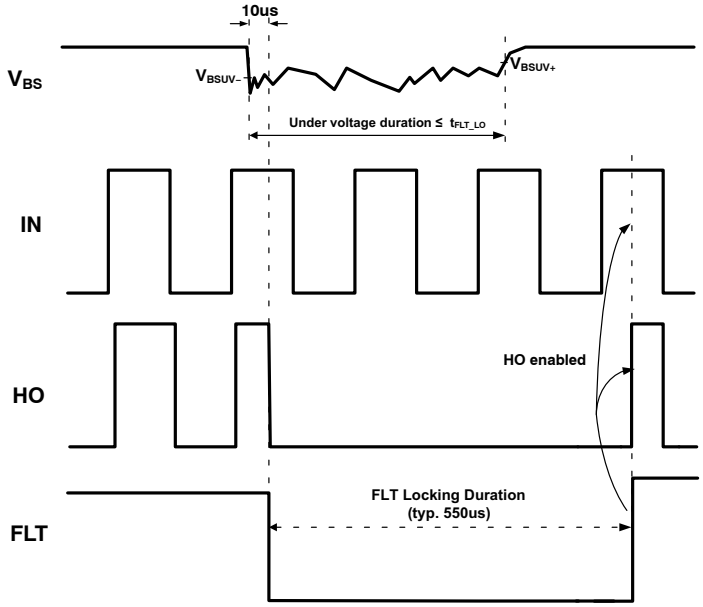


Figure 17. Under−Voltage Condition Shorter than FLT Locking Duration

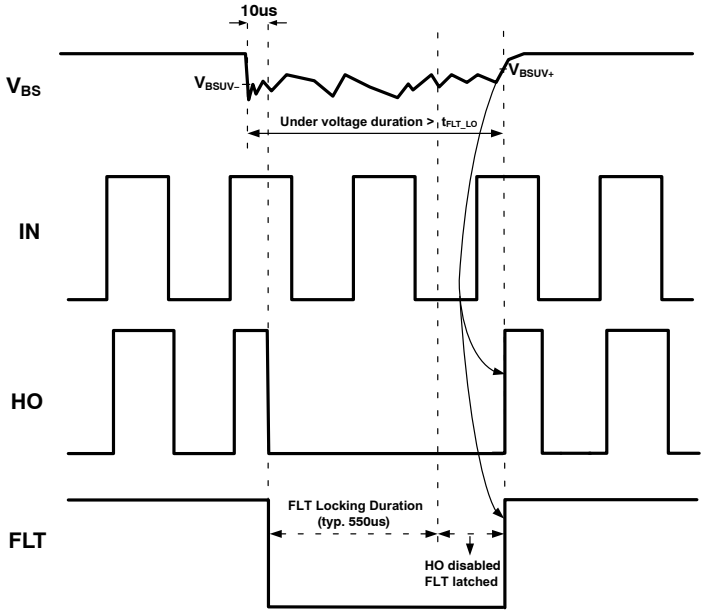


Figure 18. Under−Voltage Condition Longer than FLT Locking Duration

Desaturation Protection with Soft Shutdown

The gate driver has a desaturation detection circuit that monitors the drain to source V_{DS} voltage of the power MOSFET through the desaturation detection pin. As shown in the simplified block diagram in Figure 2, the desaturation circuit comprises of:

- An internal current source that provides a continuous current toward the power stage to monitor the V_{DS} voltage. The desat current source (I_{DESAT}) is supplied from the V_B pin and is continuously active as soon as the V_{DD} is higher than the $UVLO_{VDD+}$, independent of the status of the input logic.
- An internal comparator that compares the voltage at the desat pin (V_{DESAT}) with the defined desat threshold ($V_{DESAT,TH}$) of 3 V (typ.). When V_{DESAT} exceeds $V_{DESAT,TH}$, the comparator simultaneously turns off the output ‘slowly’ and triggers a fault condition by pulling down the fault pin internally.

As shown in application schematic in Figure 1, the desat diode D_1, resistor R_1, blanking capacitor C_{BL}, and P−channel JFET P_1 are the minimum external components required to operate the desaturation protection scheme. The driver needs an external pull down transistor P_1 to discharge I_{DESAT} and C_{BL} as soon as the driver output turns off.

Otherwise, the blanking capacitor will continue to charge up and eventually trigger desat. The presence of a normally on P1 also enhances noise immunity of desat blanking capacitor against false triggering during the turn on event of complementary power switch. The external desat components can be modified to adjust the blanking time and the desat detection threshold for a given application. It is recommended to refer to the Application Note for more details.

If the power switch is turned−off rapidly during a heavy−load condition, the high currents may generate a voltage overshoot across the power switch that could potentially damage it. In order to protect the devices, the driver has a soft shutdown feature, which activates upon desat detection. The output is then driven low through a large turn−off resistance (R_{SOFT}) which provides a significantly higher resistive path for the gate capacitance to discharge than during the regular turn−off process. As a result, the possibility of an abrupt overvoltage spike on the power switches is reduced.

When the voltage at the desaturation pin exceeds the defined desat threshold, following protection sequence is performed:

- The gate driver initiates a soft shutdown. The driver will provide a high resistive path through R_{SOFT} for gate capacitance to discharge slowly [see Figure 19]. The fall rate of HO is determined by the time constant of the RC discharge path.
- The driver also triggers an internal fault and pulls down the fault pin for the period equivalent to Fault Locking duration (typ. 550 μs).

NOTE: If the desat condition persists even after the fault locking duration, and if the input signal is still provided, the driver output will reappear for a period equivalent to the blanking time, after which the desat protection will retrigger the soft shutdown and turn off the output again.

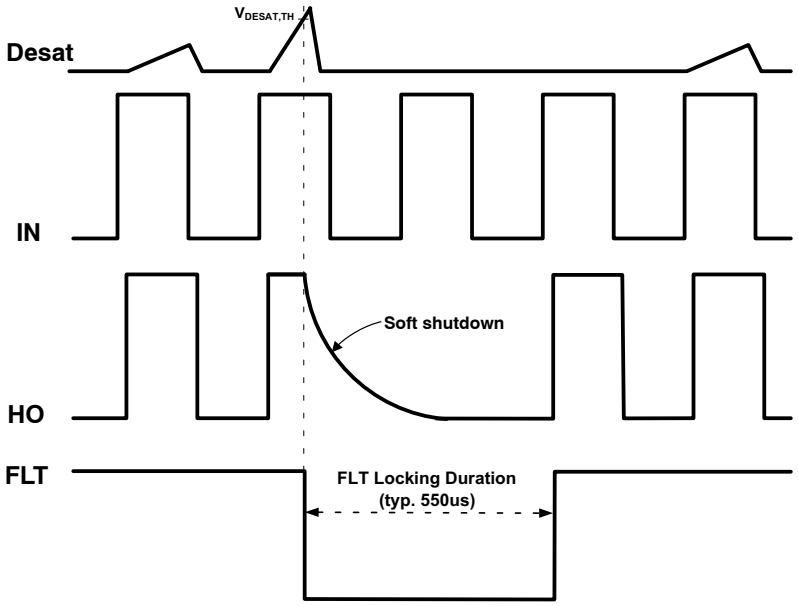


Figure 19. Desaturation Protection and Soft Shutdown

External Fault Triggerring

The FLT pin is bi−directional in nature and is in a pulled−up state for normal operation. The gate driver pulls down the FLT pin internally during desat and under−voltage lockout condition. As shown in Figure 20, if the FLT pin is externally pulled down to a logic low for a period longer than the external FLT pulse width (min. 3 μs), the driver turns off. It is important to note that the FLT locking duration is not valid for external fault trigger condition. As a result, the output is reactivated as soon as the FLT pin is released (set to logic 1). In this case, the FLT pin performs similar to an enable pin. The external fault triggering capability allows the interconnection of fault pins of multiple gate drivers on both high side and low side driver stages. For example, in a multi−phase inverter system, the fault pins of all high−side drivers (or low−side drivers) could be tied together and controlled with an external controller to achieve Active short−circuit (ASC) protection. It is recommended to refer to the Application Note for more details.

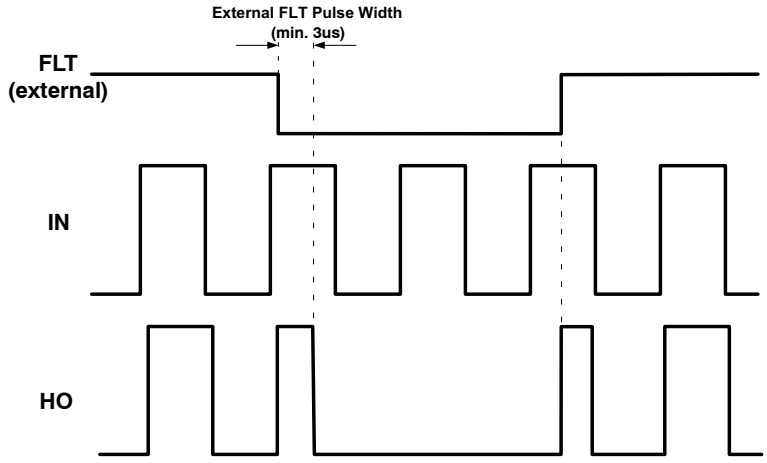


Figure 20. External fault Triggering Condition

Charge Pump for 100% Duty Cycle Operation

The FAD3171MXA driver contains an internal charge pump that enables 100% duty−cycle operation of high−side power switches. When the high−side switch is kept on for a long duration, the bootstrap capacitor could slowly discharge and may eventually trigger the under−voltage lockout protection and turn off the driver output. Therefore, the purpose of the charge pump is to supply the V_{BS} quiescent current necessary for the high−side gate driver to operate under 100% duty cycle and to compensate for additional leakage current on the gate path.

It should be ensured that the total leakage current in the gate path does not exceed the maximum output current capability of the charge pump $I_{CP,OUT}$. For example, in Figure 21, when the gate is continuously high, the pull−down resistance R_2 will continuously sink a current and for this reason, its value should be high enough to minimize the total leakage current drawn from the charge pump. Considering a maximum output current of 150 μA at $V_{BS} = CP_{ON} = 15$ V, the value of R_2 should be higher than 100 kΩ to maintain a steady charge pump output.

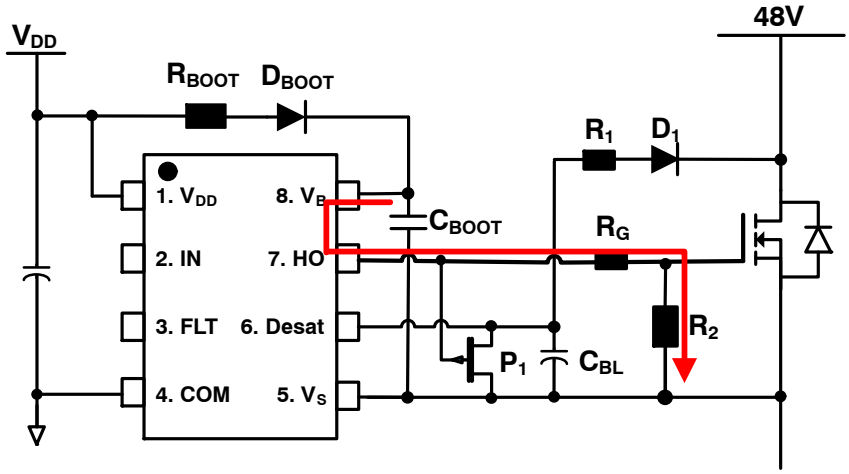


Figure 21. Leakage Current in the Gate Path

It is important to note that the charge pump is not intended to provide gate charge during switching of power MOSFET; rather its purpose is to only keep the MOSFET turned on. For this, it should be ensured at the system level that the high−side MOSFET is not operated at very high duty cycle or, if a high duty cycle operation is required, the off time should be long enough to allow the bootstrap capacitor on high−side gate driver to completely recharge.

In order to minimize continuous power dissipation, the charge pump turns on only when needed, and remains off at other times. The necessary conditions for the charge pump in FAD3171MXA to activate are:

- The V_{DD} voltage is higher than the V_{DD} under voltage positive−going threshold (V_{DDUV+})
- The V_S voltage is higher than $V_{S,CP}$ (24 V min.); below this voltage, the efficiency of the charge pump is reduced.
- The V_{BS} voltage decreases below the charge pump turn on threshold (CP_{ON}).

The charge pump deactivates as soon as:

- The V_{BS} voltage rises back to a value higher the charge pump turn off threshold (CP_{OFF}).
- The V_{DD} is lower than the V_{DD} under voltage negative−going threshold (V_{DDUV-}).

In order to ensure that the charge pump and the UVLO function do not interfere with each other, the charge pump turn−on threshold (CP_{ON}) is designed to be higher than the V_{BSUV-} threshold. As a result, the driver output is higher than the V_{BSUV-} threshold during charge pump mode. If the load on the charge pump exceeds $I_{CP,OUT}$, the voltage across the V_B−V_S pins will slowly decrease and eventually trigger the under−voltage lockout protection and turn off the driver output.

Switching Time Definitions

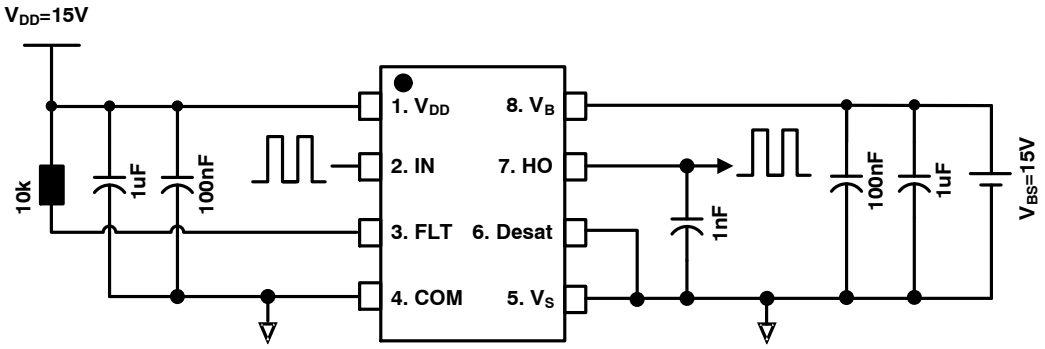


Figure 22. Switching Time Test Circuit

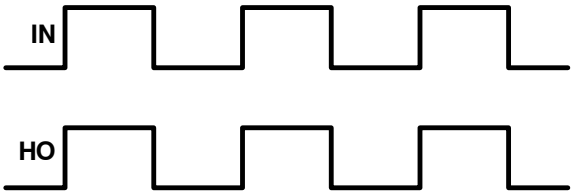


Figure 23. Input / Output Timing Diagram

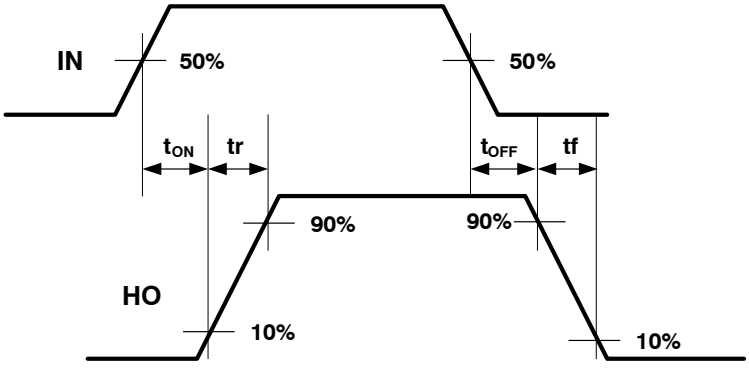
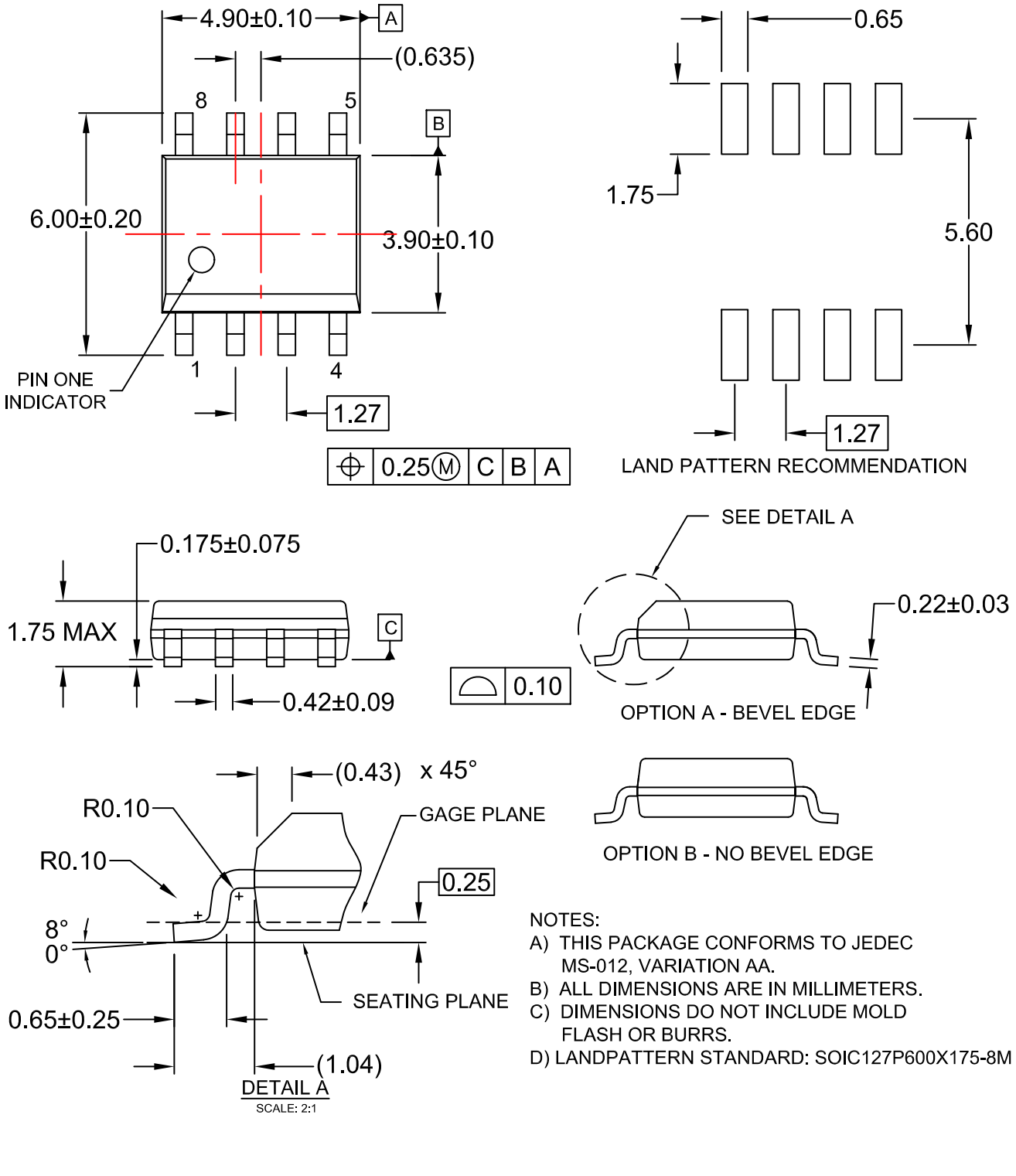


Figure 24. Switching Time Waveform Definitions

PACKAGE DIMENSIONS

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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