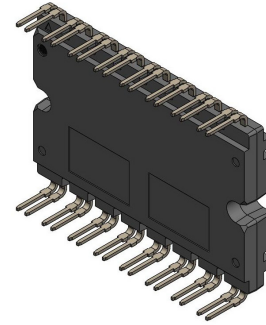


Introduction to 1200 V SiC MOSFET Modules for On-Board Charger Applications: NVXK2KR80WDT, NVXK2TR80WDT, & NVXK2TR40WDT



AND90017/D

Summary

As the trend in electric vehicle On-Board Charger (OBC) design moves rapidly to higher power and higher switching frequency operation, the demand for SiC MOSFETs for this application is also growing. Many high voltage discrete SiC MOSFETs are already in the marketplace and engineers are designing OBC systems to take advantage of their performance benefits. It is also noted that the changes in the PFC topology are remarkable. Designers are adopting the Bridgeless PFC topology using the SiC MOSFET due to its superior switching performance and small reverse recovery characteristics. Employing a SiC MOSFET module is known to provide benefits in terms of electrical and thermal performance as well as power density. onsemi has shown outstanding performance in the automotive module design area using Si MOSFET technology and now initiates a line of SiC MOSFET modules to enable OBC design improvements, including a PFC and DC/DC modules using 1200 V SiC devices. In this application note, these modules are introduced, and guidance is provided for employing this new line of modules.

Module Introduction

Figures 1 and 2 show uni-directional and bi-directional OBC circuit topologies that are among those receiving significant attention in the EV market. onsemi's new line of transfer molded, high voltage isolated multi-chip modules is introduced with three initial members of the family:

- NVXK2KR80WDT Vienna rectifier module featuring 1200 V 80 mΩ SiC MOSFET and SiC and Si diodes mounted on Al₂O₃ ceramic substrate,
- NVXK2TR80WDT dual half bridge module featuring 1200 V 80 mΩ SiC MOSFETs mounted on Al₂O₃ ceramic substrate, and
- NVXK2TR40WXT dual half bridge module featuring 1200 V 40 mΩ SiC MOSFETs mounted on AlN ceramic substrate for increased current handling capability.

Summary package information and schematics for these three modules are given in Figures 3 and 4.

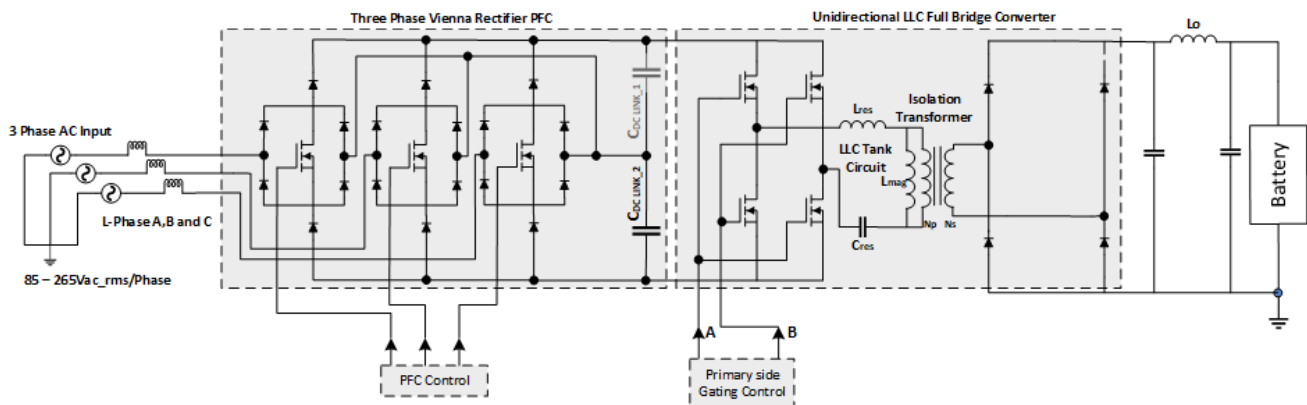


Figure 1. Typical Module Application: Uni-Directional On-Board Charger with Vienna Rectifier PFC Stage

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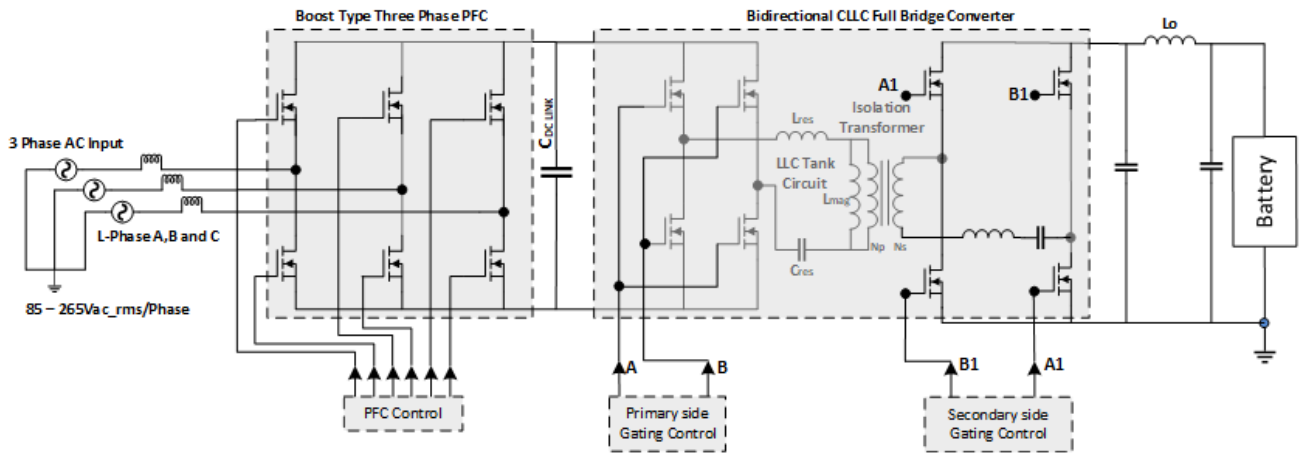


Figure 2. Alternative Module Application: Bi-Directional On-Board Charger Using Multiple Half-Bridges

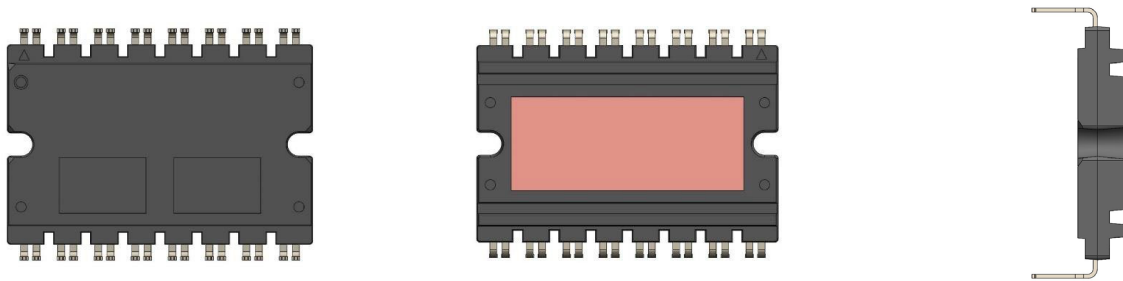
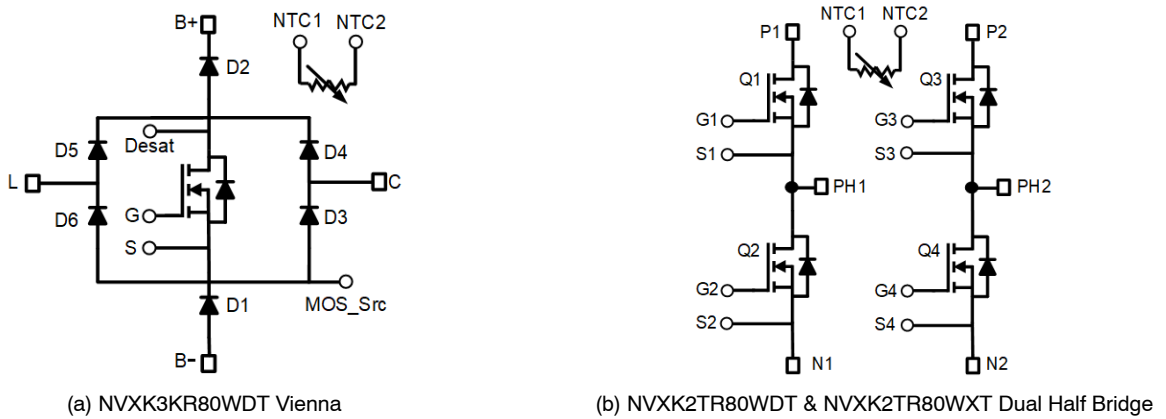


Figure 3. 1200 V SiC MOSFET Module Package Outline



(a) NVXK3KR80WDT Vienna

(b) NVXK2TR80WDT & NVXK2TR80WXT Dual Half Bridge

Figure 4. Module Design Variations

APPLICATIONS INFORMATION

Significant design resources are available from **onsemi** and from the open technical literature which will aid the automotive OBC designer to properly use SiC MOSFETs in various circuit topologies. These include the following resources available from www.onsemi.com:

- AND90103/D **onsemi** M1 1200 V SiC MOSFETs and Modules: Characteristics and Driving Recommendations
- HDBK853/D Power Factor Correction Handbook
- AND90061/D Half-Bridge LLC Resonant Converter Design Using NCP4390/NCV4390
- TND6318/D On Board Charger (OBC) LLC Converter
- AND9957/D On Board Charger (OBC) Three-Phase PFC Converter
- EVBUM2731/D 6.6 kW On Board EV Charger (SiC Model) Evaluation Board User’s Manual
- EVBUM2784/D 6.6 kW Totem-Pole Demo Board User’s Manual

Guidance is also available to aid practicing engineers in the modeling aspects of developing a complex system such as an automotive OBC:

- AND9783/D How to Use Physical and Scalable Models with SIMetrix, OrCAD, and LTSpice
- AND90096/D Usage of SIMetrix to Study MOSFETs Thermal Behaviors on Heatsink

The reader is also encouraged to review available application notes from **onsemi** that provide useful information on related products with respect to mechanical mounting and PCB design:

- AND9922/D ASPM27 Series Package Assembly Guidance
- AND90036/D DIP-26 Series: New Transfer Molded Power Integrated Module (TMPIM) for Industrial Drives (pages 8ff)

A fine paper by Thangavela, et al, regarding the Vienna topology of the PFC is cited in reference [1], as well as a master’s thesis by Yutong Zhu of the University of Wisconsin-Madison [2].

In this application note, we will focus on the technical details of the **onsemi** 1200 V SiC MOSFET modules that can be employed to implement the OBC power stages that are described in detail in the above references.

Current and Voltage Ratings

Drain-source breakdown voltage rating for all the subject SiC MOSFET modules is $BV_{DSS} = 1200\text{ V}$, guaranteeing a minimum breakdown of 1200 V across the operating junction temperature range -40°C to 175°C .

Gate-source voltage has a maximum safe range of $+25\text{ V}/-15\text{ V}$, while the recommended operating voltage range is $+20\text{ V}$ for turn on and -5 V for turn off. These values are consistent across all three part numbers.

Current ratings as provided in the data sheet maximum ratings tables reflect the qualification of these modules

according to ECPE Guideline AQG 324 [3]. This value tends to be a little more conservative than the traditional discrete MOSFET I_D continuous rating, which is a purely algebraic determination based on $R_{DS(on)}$ at $T_{J(max)}$ and the thermal resistance value $R_{\theta JC}$, as given in equation 1.

$$I_D = \sqrt{\frac{T_{J(max)} - T_C}{R_{DS(on)[T_{J(max)}} \cdot R_{\theta JC}}} \tag{eq. 1}$$

In the associated data sheets, the user can refer to Figure 10 to see the maximum drain current as a function of case temperature, as given in equation 1. Because the data sheet current rating information is only representative of the data sheet conditions, it is recommended that the user consider using circuit simulation that is specific to his/her system design to evaluate more closely the thermal and loss performance of the modules in their specific application.

Package Thermal Performance

onsemi utilizes computational fluid dynamics software to analyze the thermal response of the module and heatsink assembly under various boundary conditions, and validates the results through testing. Figure 5 shows the concept for analyzing the $Z_{\theta JC}$ and $Z_{\Psi JS}$ thermal impedance characteristics. For $Z_{\theta JC}$, the module bottom surface is maintained isothermal at 100°C , while for the $Z_{\Psi JS}$ characteristic, the boundary conditions are as shown in Figure 5, that is, specific TIM thickness and conductivity, aluminum heatsink, and isothermal surface. The thermal characteristics provided in the module data sheets reflect the results of this combined, validated test and analysis process.

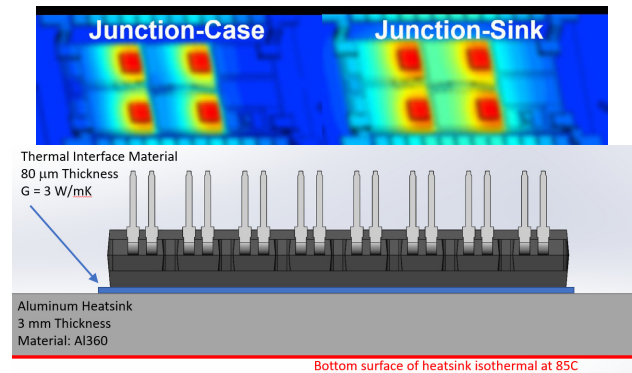


Figure 5. Thermal System Concept and Example Results

For the 5-pin bare die models of the MOSFETs, thermal performance can be observed in simulation by employing a Cauer thermal network connected to the TC terminal on one end, and a reference power supply set to the system variable {temp} to represent the ambient or heatsink temperature. The data sheet provides the Foster network RC values for the thermal equivalent circuit; Table 1 provides the Cauer network equivalent RC values.

As an example, the circuit in Figure 6 is used in SIMetrix to simulate the 80 mΩ bare die with a simple excitation to cause heating, and the above-referenced Cauer network for the NVXK2TR40WXT module. This is shown with constant DC drain current near the thermal limit of the package, with a gate voltage $V_{GS} = 20$ V. This demonstrates the connections to the Cauer network and verifies the data sheet I_D limit shown in Figure 10 of the data sheet, with a case temperature of 25°C.

Table 1. CAUER NETWORK FOR THERMAL IMPEDANCE, $Z_{\theta JC}$

Node #	NVXK2xx80WDT		NVXK2TR40WXT	
	R, Ω	C, F	R, Ω	C, F
1 (T_C)	0.0192	4.539e-4	0.012	7.943e-4
2	0.1148	5.580e-4	0.0528	8.656e-4
3	0.4069	5.30e-3	0.2516	7.23e-3
4	1.2544	33.4e-3	0.131	0.2026
5	0.0410	4.819	5.733e-3	31.539
6 (T_{REF})	0.0034	27.015	3.599e-3	140.487
$R_{\theta JC}$	1.84°C/W	~	0.47°C/W	~

The temperature response results shown in Figure 7 show DC current values of 65, 66, 67, 68, and 69 amps. The voltage response represents temperature of the junction in °C. This can be compared directly to Figure 10 of the data sheet for NVXK2TR40WXT to see that the limit of 68 A is consistent with the simulation.

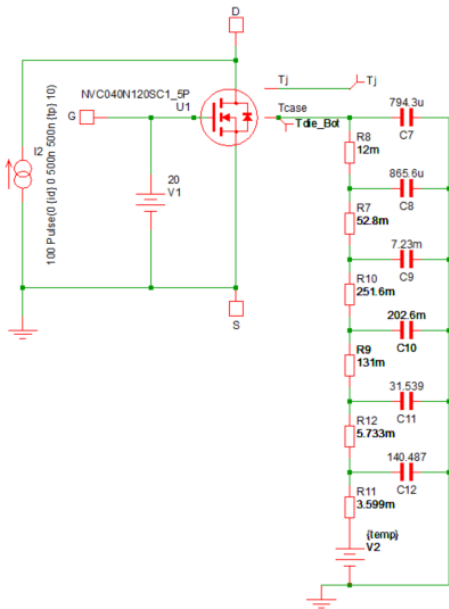


Figure 6. Example Cauer Network with 40 mΩ Die

Should a user have a thermal stack similar to that shown in Figure 5 for the junction-sink, the “normalized”

junction-sink Cauer network thermal resistances (R_n) and thermal capacitances (C_n) are given in Table 2 for the NVXK2xx80WDT and NVXK2TR40WXT modules. To convert this Cauer network to a “de-normalized” network representing either the data sheet value for $R_{\Psi JS}$ or a customer-specified value, simply multiply the R_n -values by the desired $R_{\Psi JS}$, and divide the C_n -values by the same $R_{\Psi JS}$, as given in equation 2. The resulting RC values will produce a transient thermal impedance curve with the proper time constants and the desired steady state value, $R_{\Psi JS}$.

$$R_i = R_{\theta JS} \cdot R_n \quad C_i = \frac{C_n}{R_{\theta JS}} \quad (\text{eq. 2})$$

To properly connect the de-normalized $Z_{\Psi JS}$ network to the SiC MOSFET model, simply replace the values of the ladder network shown in Figure 6 for the $Z_{\theta JC}$ characteristic with the values computed using equation 2 and the system will produce the thermal response according to $Z_{\Psi JS}$.

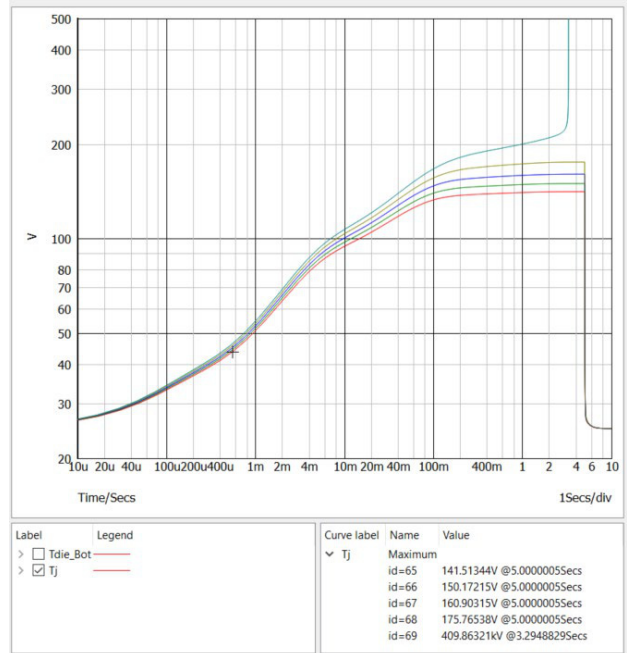


Figure 7. Temperature Response to Range of DC Current

Table 2. CAUER NETWORK FOR NORMALIZED THERMAL IMPEDANCE, $Z_{\Psi JS}$

Node #	NVXK2xx80WDT		NVXK2TR40WXT	
	R, Ω	C, F	R, Ω	C, F
1 (T_C)	2.265e-3	1.379e-3	2.332e-3	1.988e-3
2	5.765e-2	1.739e-3	4.073e-2	2.458e-3
3	0.2109	1.022e-2	1.579e-2	1.579e-2
4	0.4959	9.365e-2	5.325e-1	8.723e-2
5	0.2222	2.347	2.762e-1	1.889
6 (T_{REF})	9.903e-3	228.5	1.221e-2	182.9
$R_{\Psi JS}$	1.0°C/W	~	1.0°C/W	~

The Cauer network RC values of Table 2 correspond to the two normalized transient thermal impedance curves shown in Figure 8. Note that the normalization process forces these curves to have steady state values of 1.0°C/W. When the “de-normalization” is carried out according to equation 2, the user will achieve the desired steady state value (for example, from the data sheet, 0.95°C/W for $R_{\psi JS}$ for NVXK2TR40WXT) and the correct dynamic behavior.

The modules include an NTC thermistor, TDK part number B57342V5103H060 [7], which has the resistance vs. temperature characteristic shown in Figure 9. Temperature can be computed, in degrees Celsius, from the resistance value based on the equation 3.

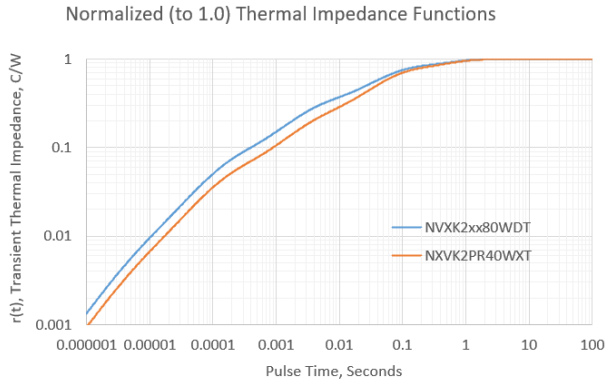


Figure 8. Normalized Transient Thermal Impedance $Z_{\psi JS}$

NTC resistance may be measured by employing a voltage divider with an external voltage source and external resistor.

$$T(R) = \frac{T_0 \cdot B}{T_0 \cdot \ln \frac{R}{R_0} + B} \quad (\text{eq. 3})$$

Where $T_0 = 298$, B is taken from the data sheet [7] (typically 3650), $R_0 = 10 \text{ k}\Omega$, and R is the measured temperature-dependent resistance. In these modules, $T(R)$ can be taken equal to the case temperature, and the Cauer network in Table 1 can be used to estimate junction temperature in real time.

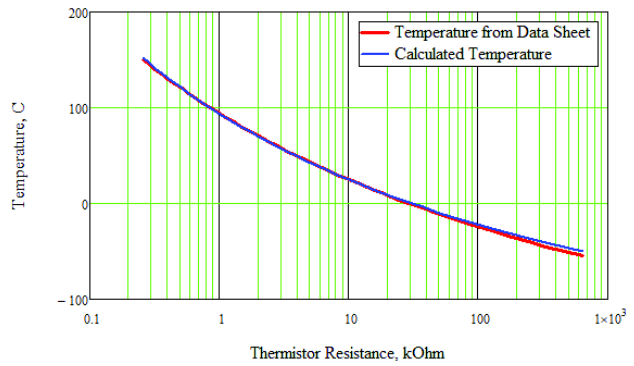


Figure 9. NTC R–T Characteristic and Temperature Computed from R with B = 3950

Simulation for Module & System Performance

Users of these devices have available to them via www.onsemi.com simulation models of the SiC MOSFET bare die that are used in the modules. These SIMetrix, pSpice, and LTSpice models can be combined with equivalent circuit models for the package to produce a very accurate simulation of the circuit behavior. This allows designers to assess the performance of the modules in a very realistic manner when combined with their gate drive circuits and any other related circuitry constituting the full OBC system.

Table 3 provides a cross reference to the die models that should be downloaded from www.onsemi.com to populate the module models. Figures 10 and 11 show the equivalent series inductance and resistance values for each path in the module between external pins and die terminals, for the dual half bridge modules and the VIENNA module, respectively. These equivalent package models are derived from a Spice model generated from the ANSYS Q3D [4] representation of the full 3D geometry and material properties of the modules.

Figure 10 represents a simplified, lumped distributed parameter model of the dual half bridge modules, NVXK2TR80WDT and NVXK2TR40DXT. The MOSFET shown in Figure 10 is the bare die model for the 80 mΩ 1200 V SiC MOSFET populating the four die locations in the module.

Table 3. MODULE DIE MODEL CORRESPONDENCE

Module Part Number	MOSFET/DIODE Model
NVXK2TR80WDT	NVC080N120SC1
NVXK2TR40WXT	NVC040N120SC1
NVXK2KR80WDT	NVC080N120SC1 FFSH20120A-F085* VS207DM..CCB*

*Detailed model not available.

Note in Figure 10 that a high value parallel resistor can be added to each series inductance to aid in convergence if such a problem should arise. These parasitic R and L values can be taken to be the same for both the 40 mΩ NVXK2TR40WXT and the 80 mΩ NVXK2TR80WDT.

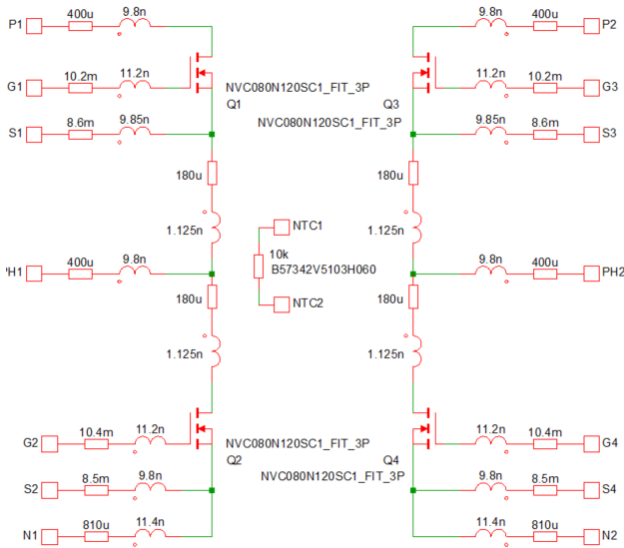


Figure 10. Simplified Package Model for Dual Half Bridge

Similarly, the Q3D model for the NVXK2KR80WDT package has been exercised to determine a lumped parameter parasitic model for the Vienna module, which is shown in Figure 11. The power devices and terminals are labeled the same as in the schematic in the data sheet. Note that all inductances are given in nH, and the resistance values (other than the NTC) are given in μΩ or mΩ. Note that this circuit is a simplification of the Q3D model, notably missing any capacitive effects, and thus will not produce all the same waveform dynamics as the real device or even the Q3D model. If a full Q3D model is desired, please contact your local onsemi sales office to enquire.

The reader can place these schematics within their Spice or SIMetrix simulation for the entire OBC system, or they can use these models combined with a representation of a simple test stand that could be constructed to test the performance of the models. The MOSFET models obtained

from www.onsemi.com can be populated as 5-pin models to include the T_J and T_C terminals. This will allow the simulation to be a coupled electro-thermal simulation and provide the highest level of accuracy for assessment of the electrical and thermal performance of the system.

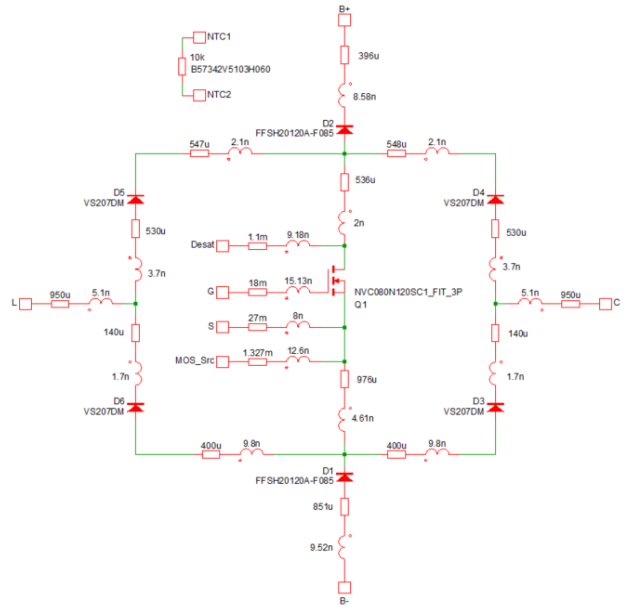


Figure 11. Simplified Package Model for Vienna Module

As an example of simulation using the combined SiC MOSFET die, module electrical parasitics, and module thermal impedance models, consider the NVXK2TR80WDT model configured in the n-pulse test circuit shown in Figure 12. Here, we have truncated the view of the schematic to show only one half of the module, e.g., one of the two half-bridges, to enable a more readable picture. An external 800 V dc supply is used to provide current to the inductive load through the half-bridge operation in the classic 2-pulse arrangement. The NVC08N120SC1_5P bare die model with T_J and T_C terminals is used, and a separate Cauer network representing the junction-to-case thermal impedance is included for each die.

Results for switching are shown in Figures 13 – 15, with a reference temperature of 25°C. Figure 13 shows the temperature profile during three sets of switching events (10 A, 20 A, and 30 A) and it is easy to see the effect of the E_{OFF} and E_{ON} during the switching events starting at 11, 23, and 35 μs, as well as the high side switch (U2) body diode losses during its off times of current recirculation.

Figure 14 shows a detail view of the 20 A turn off event for Q2, the low side MOSFET, while Figure 15 shows the subsequent 20 A turn on event. Dynamic variations in gate and drain waveforms can be seen as they are affected by stray inductances.

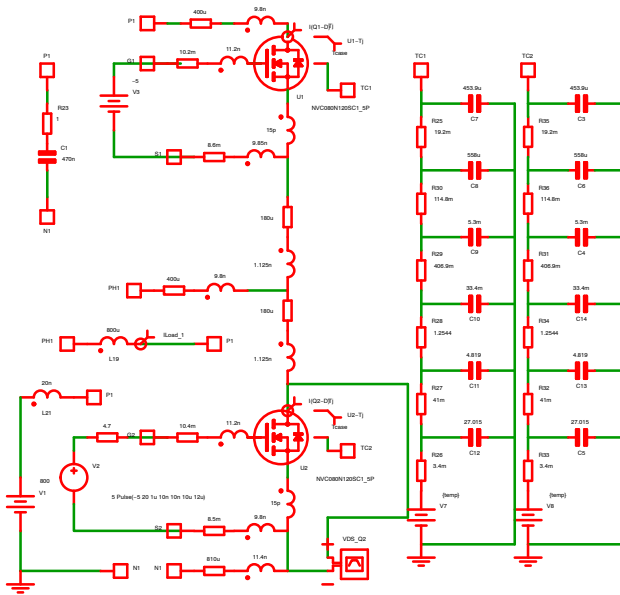


Figure 12. n-Pulse Circuit – Half of NVXK2TR80WXT

Module Electrical Isolation and Mounting Guide

Creepage and Clearance

Electrical isolation is closely related to the safety and reliability of the module in an application. IEC60664-1 [5] is the generally accepted guideline for determining minimum safe values for creepage and clearance distances under varying material classes, pollution degrees, elevations, and working voltages, to insure proper electrical isolation. The distance along a continuous insulating surface between two conductive materials is defined as creepage, and clearance is the linear distance through air between two surfaces at different potentials. The basis for the determination of a creepage distance is the rms value of the working voltage between the two conductive parts.

Refer to Tables F.2, F.4, and A.2 in [5] to determine the clearance for transient over voltages, the creepage distance to avoid tracking failure, and the altitude correction factors for clearances.

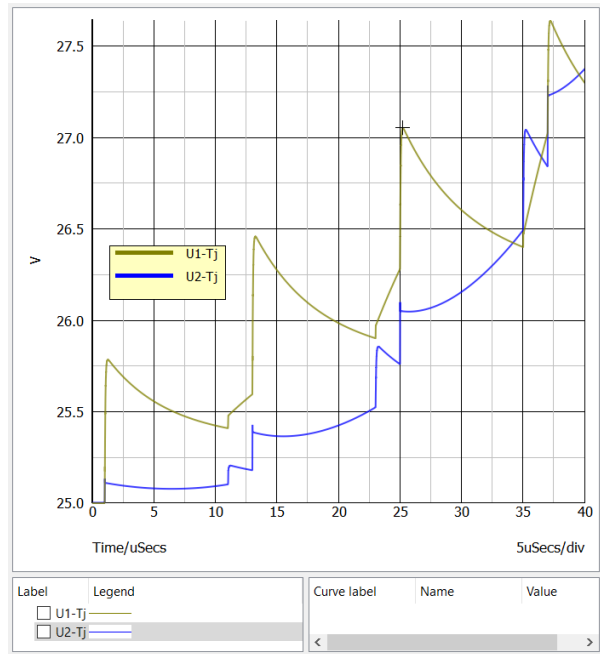


Figure 13. Temperature Response of Q1 & Q2

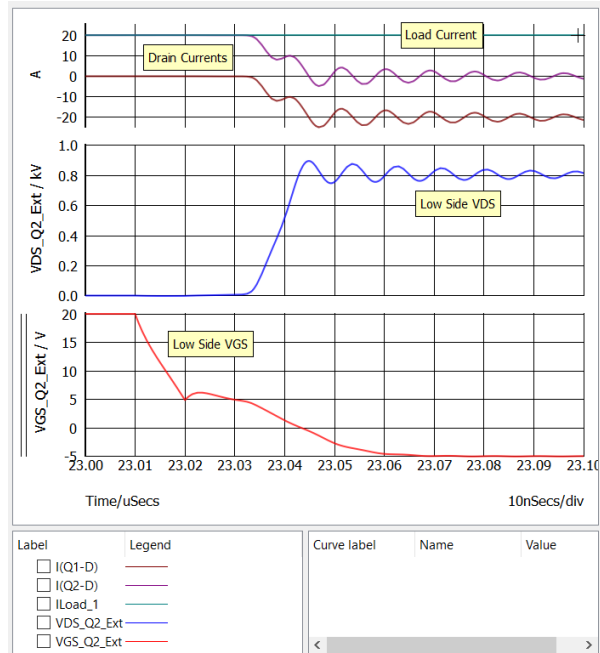


Figure 14. 20 A Q2 Turn Off Waveforms

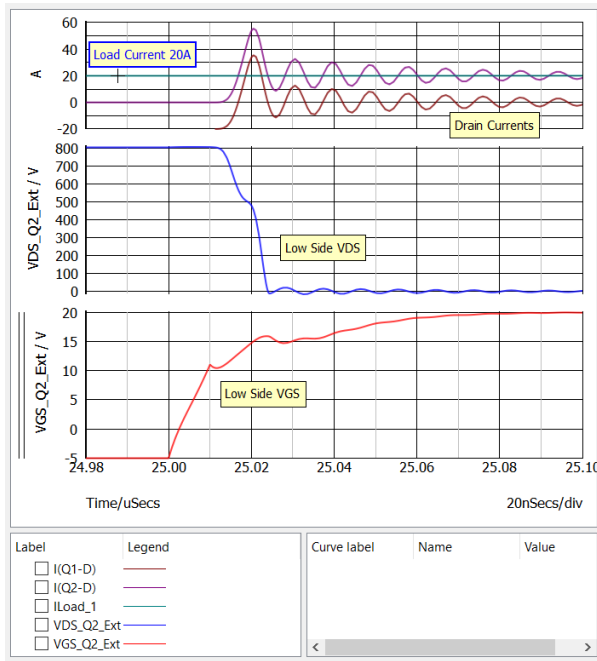


Figure 15. 20 A Q2 Turn On Waveforms

To select the proper entries in these tables, we define the working voltage as 1000 V, the transient overvoltage as 2500 V, the material group I (epoxy mold compound with comparative tracking index CTI > 600), and pollution degree 2, using the Case A (inhomogeneous field). These conditions yield the following parameters from IEC60664-1:

- Minimum Creepage Distance (F.4) = 5.0 mm
- Minimum Clearance (2000m ASL, F.2) = 1.5 mm
- Altitude Correction Factor (5000m ASL, A.2) = 1.48
- Total Clearance Required = 1.5 mm x 1.48 = 2.22 mm

The OBC modules have been designed to achieve sufficient creepage, as illustrated in Figure 16. Observing the red colored surface of the epoxy mold compound (EMC), we can see that a minimum of 12.1 mm of creepage can be achieved, allowing for variation in production placement of the heatsink, indicated by the blue arrow.

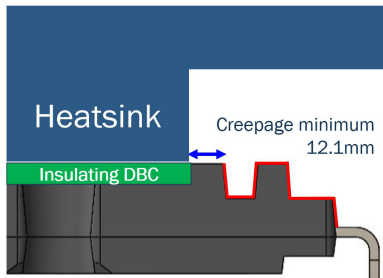


Figure 16. Illustration of Achievable Creepage

Figure 17 illustrates the clearance inherent to the design of the module. A minimum clearance of 3.3 mm is given

from the shoulder of the pins to the top surface of the EMC, which is as close as any heatsink surface might come. This is illustrated with the solid blue arrow. In a practical heatsink design with a shoulder as shown in Figure 16 to achieve higher creepage, greater than 3.3 mm clearance is possible, as shown with the dashed blue arrow.



Figure 17. Illustration of Achievable Clearance

Mounting Guide

In general, two methods of mounting the module into the user’s system are illustrated in Figure 18. Simply put, the module can be mounted first to the heatsink and then to the PCB, or first to the PCB and then to the heatsink. It is recommended to follow Method 1, mounting to the PCB first and then to the heatsink, to allow the use of standard soldering processes and avoid selective soldering operations.

When mounting the module to a heatsink, users should follow the recommendations in Table 4 to avoid mechanical damage to the module, especially due to applying excessive torque to the mounting screw. With the specified torque application, the size of the drilled holes in the heatsink should be exactly matched to the specification for the screw, and the surface of the heatsink should be smoothed by removing burrs and protrusions to satisfy the flatness and roughness requirement. The definition of flatness and roughness on heatsink surface are illustrated in Figure 19. Table 4 shows the guideline for the mounting torque (assuming a SEMS-type M3 screw with washer), flatness of the surface of the heatsink and the DBC surface, and the roughness of the heatsink surface.

Table 4. MOUNTING TORQUE AND FLATNESS GUIDELINE

Item	Limits			Units
	Min	Typ	Max	
Mounting Torque (M3)	0.6	0.65	0.8	Nm
DBC Flatness	0	40	120	µm
Heatsink Flatness	-100	-	50	µm
Heatsink Roughness	0	-	10	µm

The module mounting sequence is described as below and illustrated in Figure 19.

- Apply thermal interface material (TIM)
- Pre-screw side A ~30% torque
- Pre-screw side B ~30% torque
- Final screw side B (full torque)
- Final screw side A (full torque)

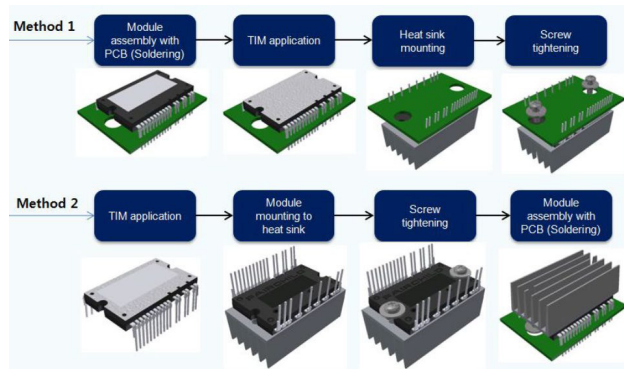


Figure 18. Mounting Methods



Figure 19. Flatness (a) and Roughness (b) of the Heatsink

Thermal Interface Material (TIM) Application

TIM is applied between the heatsink and the module to reduce the contact thermal resistance. User should make sure that the TIM is applied thinly and evenly based on the TIM datasheet including the thickness [m] and thermal conductivity, [W/mK]. Only a small amount of compound is required to fill the gap space between the metal contact

increasing the effective surface area for heat transfer. Since the contact surfaces are not perfectly flat, multiple air gaps can form between two solid contact surfaces. Air is a poor heat conductor preventing the heat transfer and limiting the effective contact area. Thermal Interface Materials (TIMs) need to be applied between the heat sink and the surface of the module to fill any air gaps and to achieve a low thermal resistance. The following are the general considerations when choosing TIM for the application. Besides its thermal conductivity, handling and rework performance are also important factors while selecting the proper TIM.

- High thermal conductivity
- Ease of distribution with low contact pressure
- Minimal thickness
- Degradation of characteristics over time
- Environmental impact
- Ease of handling during application or removal

Although many thermal interface materials with various properties are available nowadays, still the most commonly used in the industry is thermal grease. Thermal greases consist of silicone or hydrocarbon oils that contain various fillers which have good surface wetting characteristics and flow easily to fill void even at low mounting pressure. Standard thermal compounds have a thermal conductivity between 2.0 – 4.0 W/m-K, while the thermal conductivity of high-end compounds is in the range of 5.0 to 9.0 W/m-K or even higher. As an alternative, high thermal conductivity graphite sheets provide improved reliability and high thermal performances as well as lower overall costs due to a simplified assembly process. However, the thermal resistance depends on the thickness of the graphite sheet and the thickness and thermal conductivity should be reviewed before the selection. One representative TIM is Electrolube HTCP (Heat Transfer Compound Plus) thermal grease [6].

HTCP is a non-curing, non-silicone heat transfer paste suitable for the application where silicones are prohibited, thus avoiding issues with silicone and low molecular weight siloxane migration. It is RoHS-2 compliant. Table 5 shows the physical properties of HTCP.

Table 5. PHYSICAL PROPERTIES OF ELECTROLUBE HTCP

Category	Results
Typical Properties	
Color	White
Base	Blend of synthetic fluids
Thermo-conductive Component	Powered metal oxides
Density @ 20°C (g/mL)	3.0
Cone Penetration @ 20°C	250
Viscosity @ 1 rpm (Pas)	101 to 112
Thermal Conductivity (Guarded Hot Plate) (W/m.K)	2.5
Thermal Conductivity (Heat Flow) (W/m.K)	1.7 (calculated)
Temperature Range (°C)	-50 to 130
Permittivity @ 1 GHz	4.2
Volume Resistivity (Ω·cm)	1 x 10 ¹⁴
Dielectric Strength (kV/mm)	42
Weight Loss after 96 Hours @ 100°C	<1.0%
Flammability	UL94 V-0 equivalent

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- [1] Thandapani Thangavelu, Paramasivam Shanmugam, Karpagam Raj, “Modelling and control of VIENNA rectifier a single phase approach.” IET Power Electronics, 2015, Vol. 8, Iss. 12, pp. 2471–2482.
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